Evaluation board for AEM20940

Description

The AEM20940 evaluation board is a printed circuit board (PCB) featuring all the needed components to operate the AEM20940 integrated circuit (IC). Please refer to the datasheet for all the useful details about the AEM20940 (Document DS_AEM20940).
The AEM20940 evaluation board allows users to test the e-peas IC and analyze its performances in a laboratory-like setting.
It allows easy connections to the TEG (Thermo Electric Generator) energy harvester, the storage element and the low-voltage and high-voltage loads. It also provides all the configuration access to set the device in any one of the modes described in the datasheet. The control and status signals are available on standard pin headers, allowing users to wire for any usage scenario and evaluate the relevant performance.
The AEM20940 evaluation board is a plug and play, intuitive and efficient tool for making the appropriate decisions (component selection, operating modes) for the design of a highly efficient
subsystem in your target application.

Applications

- TEG harvesting
- Industrial monitoring
- Smart agriculture
- Home automation

Features

Four two-way screw terminals
- Source of energy (TEG)
- Low-voltage load
- High-voltage load
- Primary energy storage element

One three-way screw terminal
- Energy storage element (battery or (super)capacitor)

One 2-pin "Shrouded Header"
- Alternative connection for the storage element

Nine 3-pin headers
- Maximum power point (MPP) configuration
- Low drop-out regulators (LDOs) enabling
- Energy storage elements and LDOs configuration
- Dual-cell supercapacitor configuration
- Start-on-battery enabling

Two 2-pin headers
- Primary battery configuration

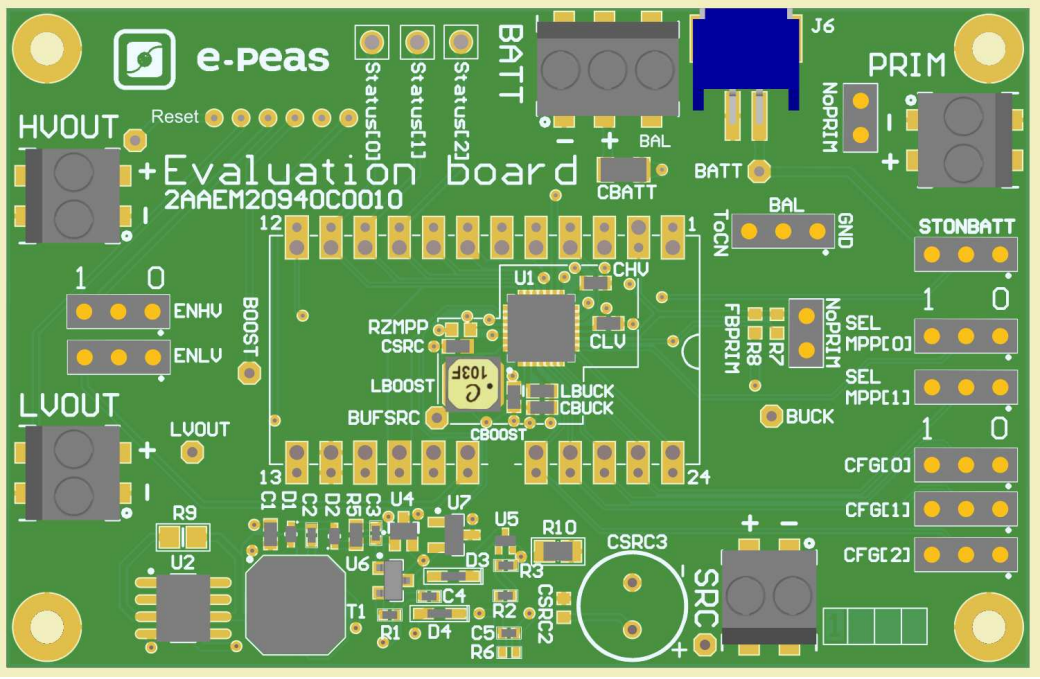
Provision for two resistors
- Primary battery configuration

Three 1-pin headers
- Access to status pins

Device information

Part number	Dimensions
2AAEM20940C0010	76 mm x 50 mm

Appearance



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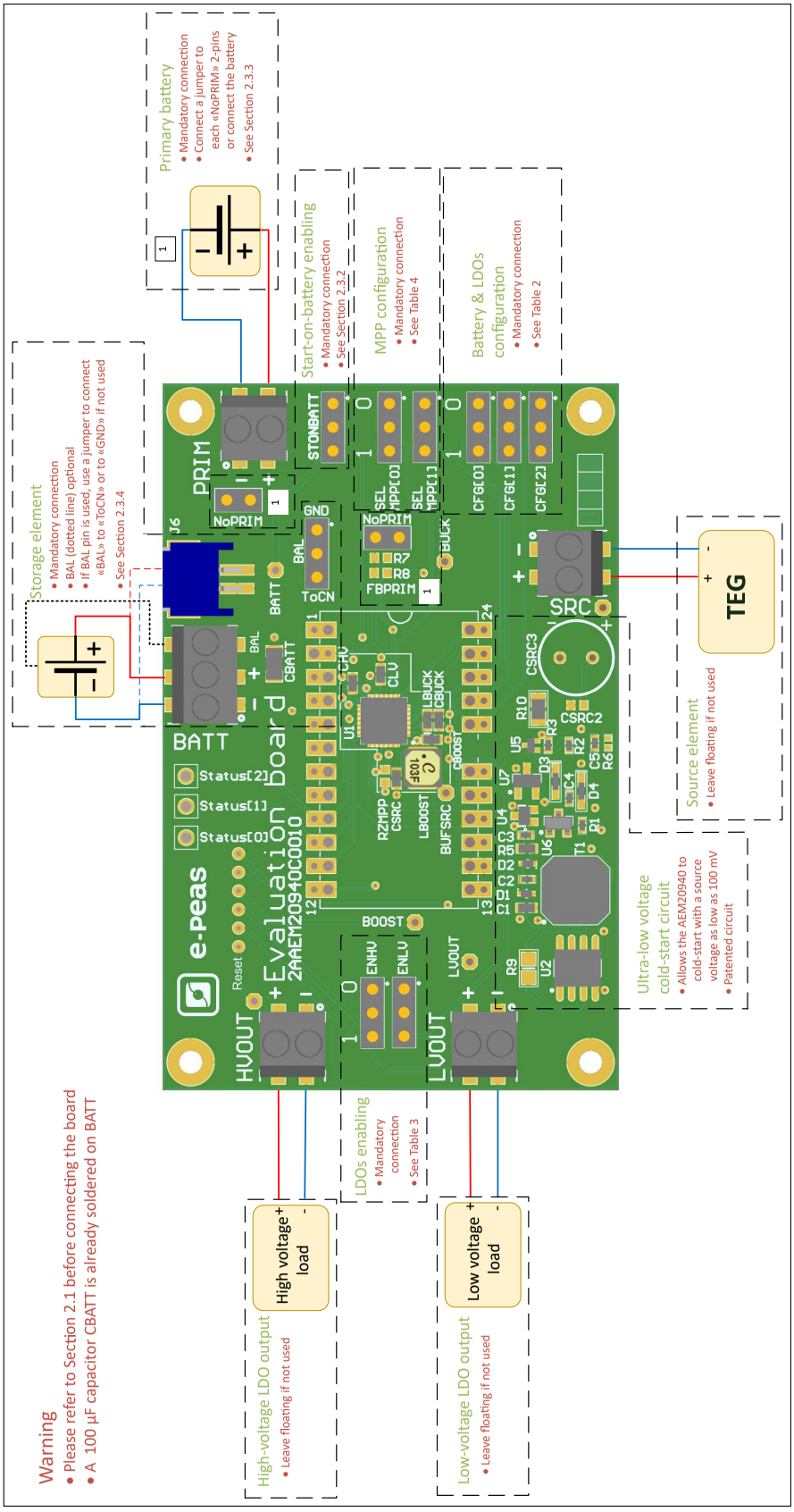


Figure 1: Connection diagram

1.1 Signals description

NAME	FUNCTION	CONNECTION	
Power signals		**If used**	**If not used**
LVOUT	Output of the low-voltage LDO regulator.	Connect a load.	
HVOUT	Output of the high-voltage LDO regulator.	Connect a load.	
BAL	Connection to mid-point of a dual-cell supercapacitor.	Connect mid-point and jumper BAL to "ToCN".	Use a jumper to connect "BAL" to "GND".
BATT	Connection to the energy storage element.	Connect storage element in addition to CBATT (100 µF).	Do not remove CBATT.
PRIM	Connection to the primary battery.	Connect primary battery.	Connect a jumper to each NoPRIM 2-pins.
SRC	Connection to the harvested energy source.	Connect the source element.	Leave floating.
Debug signals			
VBOOST	Output of the boost converter.		
VBUCK	Output of the buck converter.		
BUFSRC	Connection to an external capacitor buffering the boost converter input.		
Configuration signals			
CFG[2]	Configuration of the threshold voltages for the energy storage element and the output voltage of the LDOs.	Connect jumper (see Table 2).	Cannot be left floating (see Table 2).
CFG[1]			
CFG[0]			
SELMPP[1]	Configuration of the MPP ratio.	Connect jumper (see Table 4).	Cannot be left floating (see Table 4).
SELMPP[0]			
FB_PRIM	Configuration of the primary battery.	Use resistors R7-R8 (see Section 2.3.3).	Connect a jumper to each NoPRIM 2-pins.
RZMPP	Configuration of the constant impedance MPP.	Use resistor RZMPP (see Section 2.3.1).	Leave floating.
Control signals			
ENHV	Enabling pin for the high-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating (see Table 3).
ENLV	Enabling pin for the low-voltage LDO.	Connect jumper (see Table 3).	Cannot be left floating (see Table 3).
Status signals			
STATUS[2]	Logic output. Asserted when the AEM performs the MPP evaluation.		
STATUS[1]	Logic output. Asserted if the battery voltage falls under Vovdis or if the AEM is taking energy from the primary battery.		
STATUS[0]	Logic output. Asserted when the LDOs can be enabled.		

Table 1: Pin description

2 General Considerations

2.1 Safety information

Always connect the elements in the following order:

1. Reset the board - see "How to reset the AEM20940 evaluation board" on page 7.
2. Completely configure the PCB (jumpers/resistors);
   - MPP configuration (SELMPP[0], SELMPP[1]) - see Table 4,
   - Battery and LDOs configuration (CFG[0], CFG[1], CFG[2]) - see Table 2,
   - Primary battery configuration (NoPRIM or R7-R8) - see Section 2.3.3,
   - LDOs enabling (ENHV and ENLV) - see Table 3,
   - Balun circuit connection (BAL) - see Section 2.3.4.
3. Connect the storage elements on BATT and optionally the primary battery on PRIM.
4. Connect the high and/or low voltage loads on HVOUT/LVOUT (optional).
5. Connect the source on SRC.

To avoid damage to the board, users are urged to follow this procedure.

2.2 Basic configurations

Configuration pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	Vovch	Vchrdy	Vovdis	Vhv	Vlv	
1	1	1	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
1	1	0	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
1	0	1	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
1	0	0	2.70 V	2.30 V	2.20 V	1.8 V	1.2 V	Single-cell (super) capacitor
0	1	1	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
0	1	0	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
0	0	1	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
0	0	0	Reserved for future use					

Table 2: Usage of CFG[2:0]

ENLV	ENHV	LV output	HV output
1	1	Enabled	Enabled
1	0	Enabled	Disabled
0	1	Disabled	Enabled
0	0	Disabled	Disabled

Table 3: LDOs enabling

SELMPP[1]	SELMPP[0]	Vmpp/Voc
0	0	50%
0	1	55%
1	0	75%
1	1	ZMPP

Table 4: Usage of SELMPP[1:0]

2.3 Advanced configurations

A complete description of the system constraints and configurations is available in Section 8 "System configuration" of the AEM20940 datasheet .
A reminder on how to compute the configuration resistors value is provided below. Calculation can be made with the help of the spreadsheet found at the e-peas website.

2.3.1 ZMPP configuration

If this configuration is chosen (see Table 4), the AEM20940 regulate Vsrc at a voltage equals to the product of RZMPP times the current available at the source SRC.

- $10\,\Omega \leq$ RZMPP $\leq 1\,\mathrm{M}\Omega$

If unused, leave the resistor footprint RZMPP empty.

2.3.2 Start-on-battery

This functionality allows to start the system on a pre-charged storage element and therefore to avoid the cold-start constraints. To use this functionality, use a jumper to connect "STONBATT" to "1"and a storage element on BATT. The storage element must be charged to a voltage higher than Vchrdy.
If unused, use a jumper to connect "STONBATT" to "0".

2.3.3 Primary battery configuration

As to the main storage element, the primary battery protection levels have to be defined. To do so, use resistors R7-R8.
By defining RP = R7+R8 ($100\,\mathrm{k}\Omega \leq$ RP $\leq 500\,\mathrm{k}\Omega$):

- R7$=\frac{\text{Vprim_min}}{4} \cdot \text{RP} \cdot \frac{1}{2.2\,\mathrm{V}}$
- R8 = RP - R7

If unused, use a jumper to short each "NoPRIM" 2-pins headers.

2.3.4 Balun circuit configuration

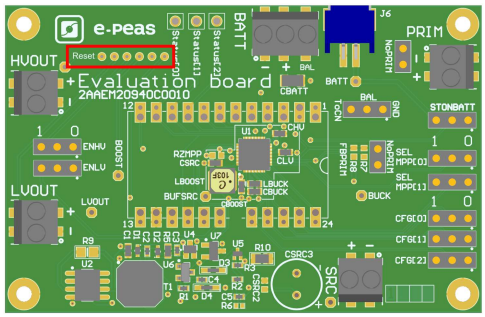
When using a dual-cell supercapacitor (that does not already include a balancing circuit), enable the balun circuit configuration to ensure equal voltage on both cells. To do so:

- Connect the node between the two supercapacitor cells to BAL (on BATT connector)
- Use a jumper to connect "BAL" to "ToCN"

If unused, use a jumper to connect "BAL" to "GND".

How to reset the AEM20940 evaluation board:

To reset the board, simply disconnect the storage device and the optional primary battery and connect the 6 "Reset" connections (working from the rightmost to the left) to a GND node (i.e. the negative pin of any connector) in order to discharge the internal nodes of the system.



3 Functional Tests

This section presents a few simple tests that allow the user to understand the functional behavior of the AEM20940. To avoid damaging the board, follow the procedure found in Section 2.1 "Safety information". If a test has to be restarted, make sure to properly reset the system to obtain reproducible results.

The following functional tests were made using the following setup:

- Configuration: SELMPP[1:0] = 00, CFG[2:0] = 100, ENLV = 1, ENHV = 1
- Storage element: capacitor (4.7 mF + CBATT)
- Load: 47 kΩ on HVOUT, LVOUT floating
- SRC: current source (5 mA) with voltage compliance (100 mV)

Feel free to adapt the setup to match your system as long as you respect the input and cold-start constraints (see Section 1 "Introduction" of AEM20940 datasheet).

3.1 Start-up

The following example allows users to observe the behavior of the AEM20940 in the wake-up mode.

Setup

1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1.

Observations and measurements

- BATT: Voltage rises as the power provided by the source is transferred to the storage element (see Figure 2).
- HLDO/LLDO: Regulated when voltage on BATT first rises above Vchrdy (see Figure 2).
- STATUS[0]: Asserted when the LDOs are ready to be enabled (refer to Section 7.2 "Normal mode" of the AEM20940 datasheet) (see Figure 2).
- STATUS[2]: Asserted each time the AEM20940 performs a MPP evaluation (see Figure 3).

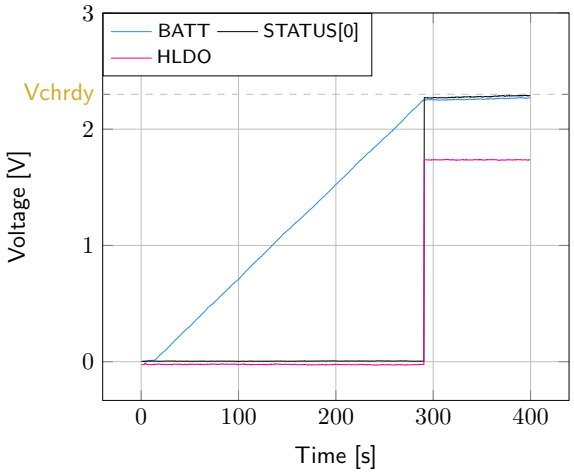


Figure 2: STATUS[0] and HLDO evolution with BATT

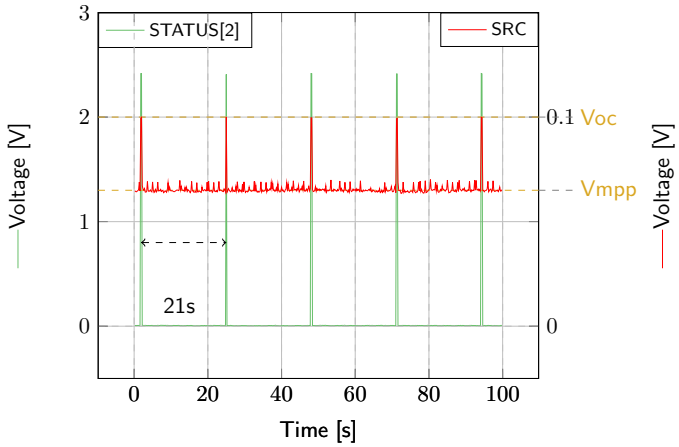


Figure 3: SRC and STATUS[2] while energy is extracted from SRC (BATT under Vovch)

3.2 Shutdown

This test allows users to observe the behavior of the AEM20940 when the system is running out of energy.

Setup

1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1. Configure the board in the desired state and start the system (see Section 3.1). Do not use a primary battery.
3. Let the system reach a steady state (i.e. voltage on BATT between Vchrdy and Vovch and STATUS[0] asserted).
4. Remove your source element and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and measurements

- BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage remains stable after crossing Vovdis (see Figure 4).
- STATUS[0]: De-asserted when the LDOs are no longer available as the storage element is running out of energy. This happens 600 ms after STATUS[1] assertion (see Figure 4).
- STATUS[1]: Asserted for 600 ms when the storage element voltage (BATT) falls below Vovdis (see Figure 4).

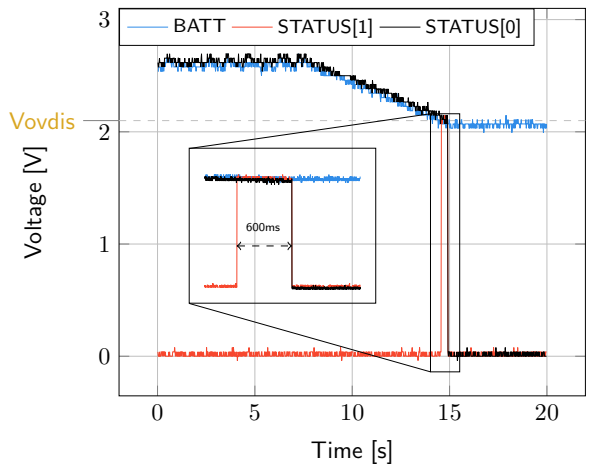


Figure 4: LDOs disabled around 600 ms after BATT reaches Vovdis

3.3 Switching on primary battery

This example allows users to observe switching from the main storage element to the primary battery when the system is running out of energy.

Setup

1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 to 5 explained in Section 2.1. Configure the board in the desired state and start the system (see Section 3.1). Connect a primary battery (example: 3.1 V coin cell with protection level at 2.4 V, R7 = 68 kΩ and R8 = 180 kΩ).
3. Let the system reach a steady state (i.e. voltage on BATT between Vchrdy and Vovch and STATUS[0] asserted).
4. Remove your source element and let the system discharge through quiescent current and HVOUT/LVOUT load(s).

Observations and measurements

- BATT: Voltage decreases as the system consumes the power accumulated in the storage element. The voltage reaches Vovdis and then rises again to Vchrdy as it is recharged from the primary battery (see Figure 5).
- STATUS[0]: Never de-asserted as the LDOs are still functional (see Figure 5).
- HLDO: Stable and not affected by switching on the primary battery (see Figure 5).

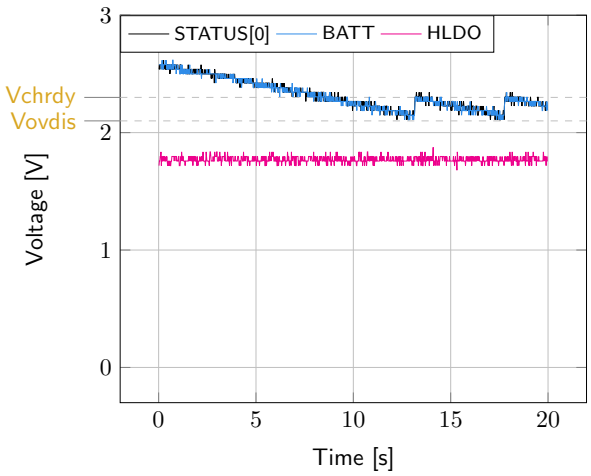


Figure 5: Switching from SRC to the primary battery

3.4 Cold start

The following test allows users to observe the minimum voltage required to coldstart the AEM20940. Be careful to avoid probing any unnecessary node to avoid leakage current induced by the probe. Make sure to properly reset the board to observe the cold-start behavior.

Setup

1. Place the probes on the nodes to be observed.
2. Referring to Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state. Do not plug any storage element in addition to CBATT.

3. SRC: Connect your source element. To match Figure 6 voltages, set the source compliance to 500 mV. This is to ease differenciating the cold start voltage (about 60 mV) from the MPP voltage (50% · 100 mV = 50 mV).

Observation and measurements

- SRC: Equals to the cold-start voltage during the cold-start phase. Regulated at the selected MPPT percentage of Voc when cold start is over (see Figure 6). Be careful that the cold-start phase time will shorten with the input power. Limit it to ease the observation.
- BATT: Starts to charge when the cold-start phase is over (see Figure 6).

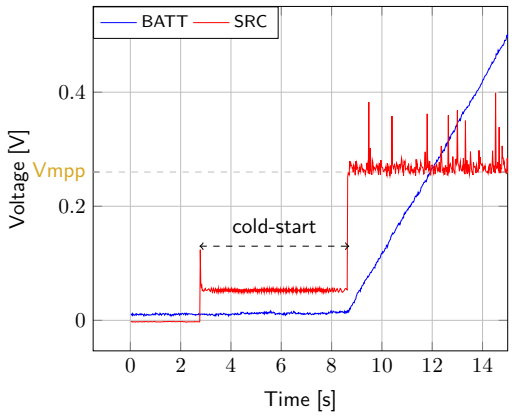


Figure 6: AEM20940 behaviour during cold start

3.5 Dual-cell supercapacitor balancing circuit

This test allows users to observe the balancing circuit behavior that maintains the voltage on BAL equilibrated.

Setup

1. Following steps 1 and 2 explained in Section 2.1 and referring to Figure 1, configure the board in the desired state. Plug the jumper linking "BAL" to "ToCN".
2. BATT: Plug capacitor C1 between the positive (+) pin and the BAL pin, and a capacitor C2 between the BAL pin and the negative (-) pin.
   Select C1 ≠ C2 such that:
   - C1 & C2 > 1 mF
   - $\frac{C2 \cdot Vchrdy}{C1} \geq 0.9\,V$
3. SRC: Plug your source element to power up the system.

Measurements

- BAL: Equal to half the voltage on BATT.

Warning regarding measurements:
Any item connected to the PCB (load, probe, storage device, etc.) involves a leakage current. This can negatively impact the measurements. Whenever possible, disconnect unused items to limit this effect.

4 Performance Tests

This section presents the tests to reproduce the performance graphs found in the AEM20940 datasheet and to understand the functionalities of the AEM20940. To be able to reproduce those tests, you will need the following:

- 1 voltage source
- 2 source measure units (SMUs)
- 1 oscilloscope

To avoid damaging the board, follow the procedure found in Section 2.1 "Safety information". If a test has to be restarted, make sure to properly reset the system to obtain reproducible results (see "How to reset the AEM20940 evaluation board" on page 7).

4.1 LDOs

The following example instructs users on how to measure the output voltage stability of the LDOs (Figure of AEM20940 datasheet).

Setup

1. Referring to Figure 1, follow steps 1 and 2 explained in Section 2.1. Configure the board in the desired state and plug your storage element(s).
2. VBOOST: Connect SMU1. Configure it to source voltage with a current compliance of 200 mA.
3. HVOUT / LVOUT: Connect SMU2 to the LDO you want to measure. Configure it to sink current with a voltage compliance of 5 V for HVOUT or 2.5 V for LVOUT.

Manipulations

1. Impose a voltage between Vovch and 5 V on SMU1 to force the AEM to start.
2. Sweep voltage on SMU1 from Vovdis + 50 mV to 4.5 V.
3. Repeat with different current levels on SMU2 (from 10 µA to 80 mA for HVOUT and from 10 µA to 20 mA for LVOUT).

Measurements

- HVOUT/LVOUT: Measure the voltage.

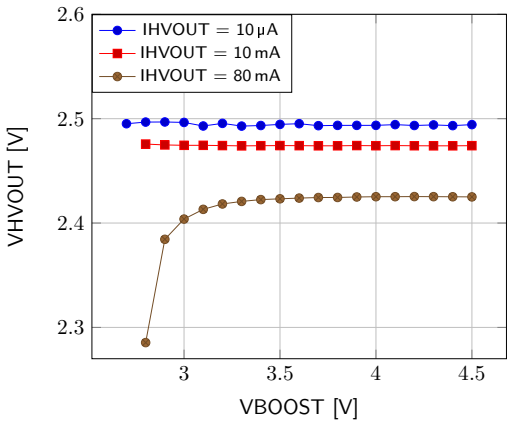


Figure 7: HVOUT at 2.5V

4.2 BOOST efficiency

This test allows users to reproduce the efficiency graphs of the boost converter (of AEM20940 datasheet).

Setup

1. Following steps 1 and 2 explained in Section 2.1 and referring to Figure 1, configure the board in the desired state.
2. VBUCK: Connect a 2.3 V voltage source to prevent VBUCK to sink from VBOOST.
3. SRC: Connect SMU1. Configure it to source current with a voltage compliance of 0 V.
4. VBOOST: Connect SMU2. Configure it to source voltage with a current compliance of 200 mA.
5. STATUS[2]: Connect to one of the SMUs to detect falling edge.

Manipulations

1. Impose a voltage between Vchrdy and 5 V on SMU2 to force the AEM to start. When done, impose a voltage between Vovdis + 50 mV and Vovch.
2. Sweep voltage compliance on SMU1 from 50 mV to 5 V.
3. Repeat with different current levels on SMU1 (from 100 µA to 100 mA) and with different voltage levels on SMU2 (from Vovdis + 50 mV to Vovch).

Measurements

- STATUS[2]: Do not make any measurements while high (boost converter is not active during MPP calculation).
- SRC: Measure the current and the voltage.

- VBOOST: Measure the current and the voltage. Repeat the measurement a copious number of times to be sure to capture the current peaks. Figure 8 has been obtained by averaging over 100 measurements configured with a 100 ms integration time.
- Deduce input and output power (P = U · I) and efficiency (η = Pout/Pin).

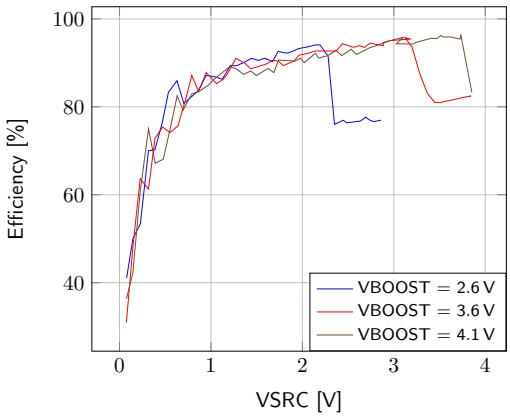


Figure 8: Boost efficiency for ISRC = 1 mA

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