DCAN500
CAN Over Powerline Transceiver

YAMAR
Preliminary *Datasheet*

1.   Overview

The DCAN500 device for CAN-BUS communication over noisy power lines (DC-CAN), supports CAN A/B protocols at speed up 500kbit/s. Multiple CAN networks may share a common DC or AC powerline where each network uses different carrier frequency. The device avoids complex cabling, saves weight and simplifies installation. Sleep mode allows low power consumption when the device is not used. The QFN32 5x5 mm package provides small PCB footprint.

The DCAN500 is beneficial for many applications using the CAN protocol but need to eliminate the CAN bus wires in Aerospace, Automotive, Industrial and more.

Applications

- Multiple vehicle CAN networks sharing the same powerline
- Aerospace CAN networks
- Sensors / actuators buses
- Robotics control network
- Truck-Trailer redundant CAN communication

Features

- Noise robust CAN A/B transceiver over DC powerline.
- CAN bitrates - 83.3kbit/s, 125kbit/s, 250kbit/, and 500kbit/s
- Multiple networks may operate over a single powerline.
- 251 selectable carrier frequencies (5MHz to 30MHz).
- Built-in CAN power line arbitration mechanism.
- Channel interference detection.
- Communicates over wide range of DC voltages.
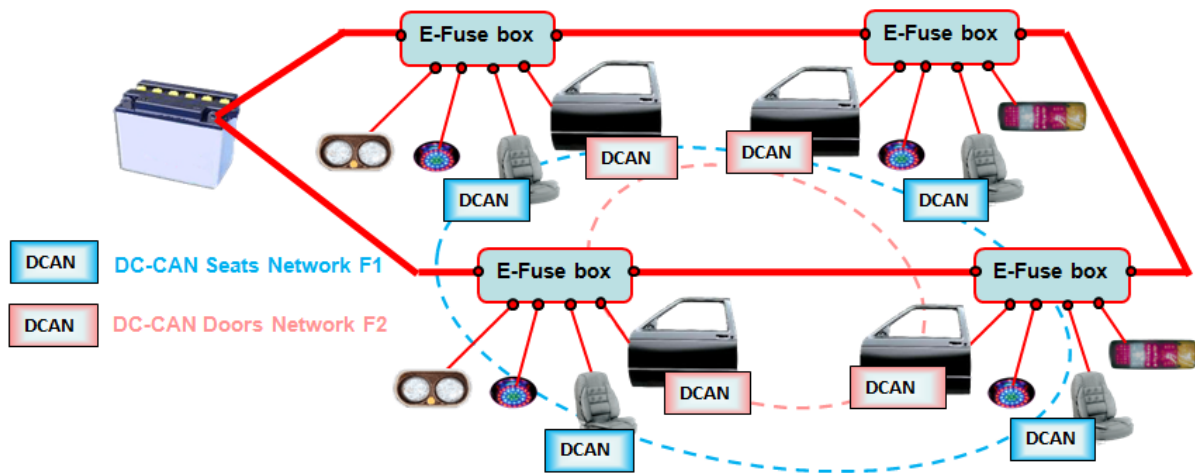- Sleep modes for low power consumption.

Figure 1- DCAN500 CAN networks sharing single powerline

TABLE OF CONTENT

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2. Description

2.1 The DCAN500 network

The DCAN500 device transmits and receives CAN messages from/to CAN controller (ECU) over DC and AC power lines at bitrates up to 500kbit/s. The device operates as part of a power line (DC-BUS) communication network consisting of multiple DCAN500 devices. The CAN messages are error protected and phase modulated by a sine wave at a user predefined carrier frequency and transmitted over the powerline as CAN frames.

All network topologies (e.g. Star, ring, line, tree, etc.) are applicable, as long as the received signal level at RXI pin is above minimal RXI_{lev} level (see 6).

Multiple DCAN500 networks can operate over single powerline, whereas each network communicates over different carrier frequency (channel).

2.2 Channel parameters

Carrier frequency: 251 selectable frequencies between 5MHz - 30MHz with 100 kHz spacing.
Powerline voltage: Any, with proper powerline coupling interfacing (see 2.5.7)
Cable length: Depends on the powerline loads AC signal-attenuation (100m is practicable)
Cable type: Any cable.

2.3 DCAN500 Architecture

Figure 2 depicts the DCAN500 blocks.
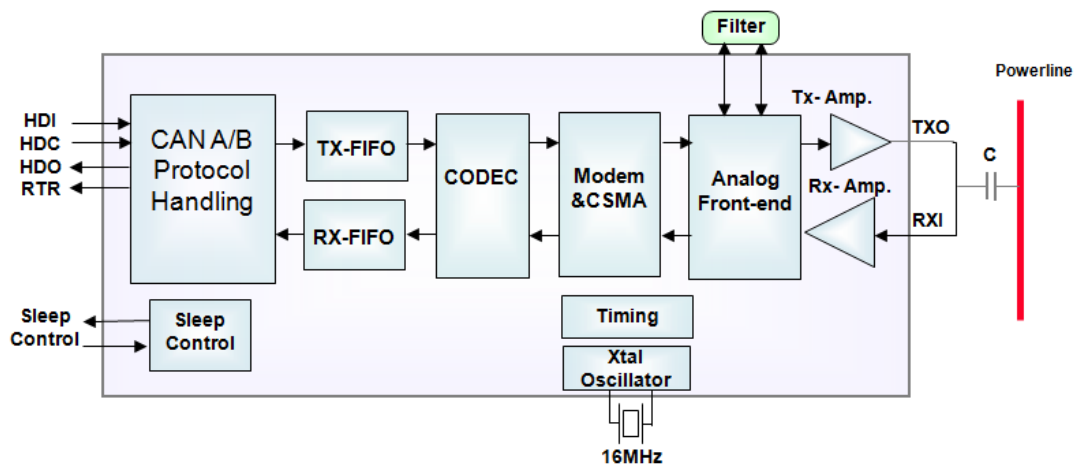
Figure 2 - DCAN500 block diagram

The DCAN500 main building blocks:

- **Protocol handling -** Interprets ECU's CAN A/B protocol.

- **Rx FIFO -** Buffers CAN frames between DCAN500 device and its ECU.

- **CODEC -** Encodes/decodes the CAN message.

- **Modem -** Phase modulates and demodulates the data to and from powerline CAN frames.

- **CSMA/CA –** CAN frame Carrier sense and arbitration mechanism.

- **Sleep -** Ensures low power consumption during Sleep mode.

2.4 Configuration and Function

2.4.1 Pinout diagram

Figure 3 - DCAN500 pinout diagram in QFN32 5x5 mm package

2.4.2 Signals and Pinout description

Table 1- Pinout description

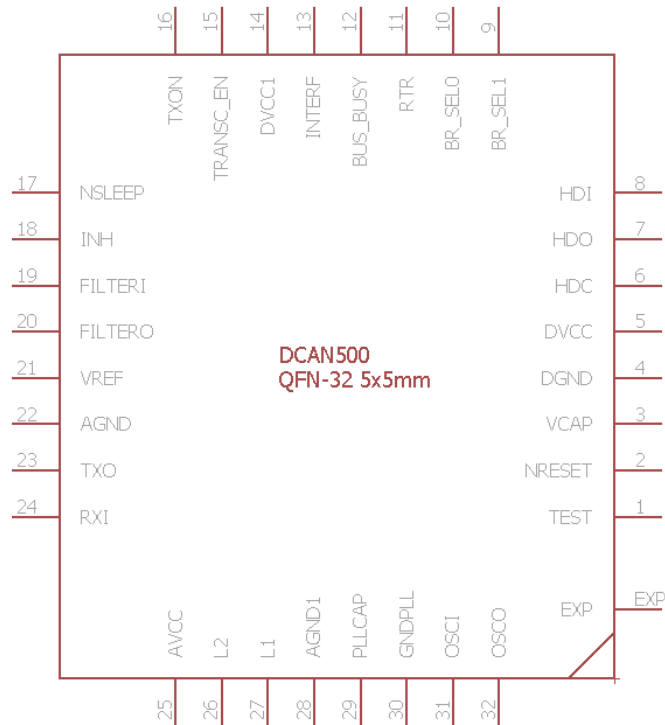| Name	Pin #	Pin type	Internal PU/PD	Description
HDO	7	Output 12mA		Outputs the received CAN data from the powerline or from internal registers to the ECU.
HDI	8	Digital input	PU	CAN message data input from the ECU to the powerline or to the internal registers.
HDC	6	Digital input	PU	ECU data/command input, enables read and write from/to DCAN500 internal control registers (see section 5.6)
TEST	1	Digital Input	PD	Test pin should be connected to Gnd.
NRESET	2	Digital Input	PU	Reset, active low.
NSLEEP	17	Digital Input		Sleep mode control input (see section 4.3). Should be pull-up to 3.3V when not in use.
BR_SEL1	9	Digital Input		ECU bit rate selection pins (sampled once after each power-up/reset event).
BR_SEL0	10	Digital Input		
RTR	11	Digital Output 8mA		Ready to Receive (Optional feature) - When high, ECU can transfer CAN messages through HDI pin. When low, ECU should pause its data bytes transfer, allowing extraction of RX-FIFO stored CAN frames to HDO pin.

BR_SEL table:

BR_SEL[1:0]	CAN Bitrate [kbit/s]
'00'	83.33
'01'	125
'10'	250
'11'	500

Name	Pin #	Pin type	Internal PU/PD	Description
TRANSC_EN	15	Digital Input	PU	Enables usage of external CAN transceiver. Normally when HDI and HDO pins connected directly to a ECU, connect this pin to GND. When HDI and HDO pins are connected to a CAN transceiver (i.e. interfacing a CAN-BUS), this pin can be left floated (see 3.1).
INH	18	Digital Output 8mA		When high, the DCAN500 is in Normal mode When low, the DCAN500 is in Sleep mode
INTERF	13	Digital Output 12mA		High while an interference signal is being detected in the operating carrier frequency.
BUS_BUSY	12	Digital Output 8mA		High when DCAN500 is transmitting over the powerline or during reception from the powerline. This function can be used to monitor the status of the powerline channel and act accordingly (wait for completion of reception or transmission).
TXON	16	Output 12mA		TX_ON output - High during transmission onto the powerline.
TXO	23	Analog Output Max 66 mA		**Powerline Transmit signal out** (see table below)
RXI	24	Analog Input		Powerline receive Input
VREF	21	Analog Output		VCC/2 analog output reference to a filtering capacitor. Place 1uF between VREF to AGND. The VREF used as virtual ground for the external analog circuitry.
FILTERI	19	Analog, Bi-directional		External filter I/O
FILTERO	20	Analog, Bi-directional		External filter I/O
OSCO	32	Analog output		16MHz Crystal Output
OSCI	31	Analog Input		16MHz Crystal Input
L1	27	Analog Input		External inductor L1 (maximal pin capacitance 1pF), see 2.5.4.
L2	26	Analog Input		External inductors L2 (optional), see2.5.4.
AVCC	25	Power		Analog 3.3V supply
AGND	22,28	Power		Analog ground
VCAP	3	Power		1.8V core supply output to a filtering capacitor. Place 4.7uF between VCAP and DGND.
DGND	4	Power		Digital Ground
DVCC	5,14	Power		Digital 3.3V supply
GNDPLL	30	Power		Analog Ground
PLLCAP	29	Power		PLL 1.8V output to a filtering capacitor. Place 1uF between PLLCAP and GNDPLL.
EXP	33	Power		Exposed pad, should be connected to DGND.

Powerline Transmit signal out (TXO, pin 23):

TXON State	REG_1[3]	TX level [V-p-p]	Impedance [Ω]
High	'0'	1	18 [1] (REG_1[0]='0')
	'1' (Default)	2	Or 36 [1] (REG_1[0]='1')
Low		High Z	200k [2]

[1] Series output impedance
[2] Input impedance referenced to VREF

PD –Internal Pull down resistor 50K Ω +/-%30
PU –Internal Pull up resistor 50K Ω +/-%30

2.5   Implementation

2.5.1   Reference schematic

Figure 4 depicts a reference DCAN500 schematic.
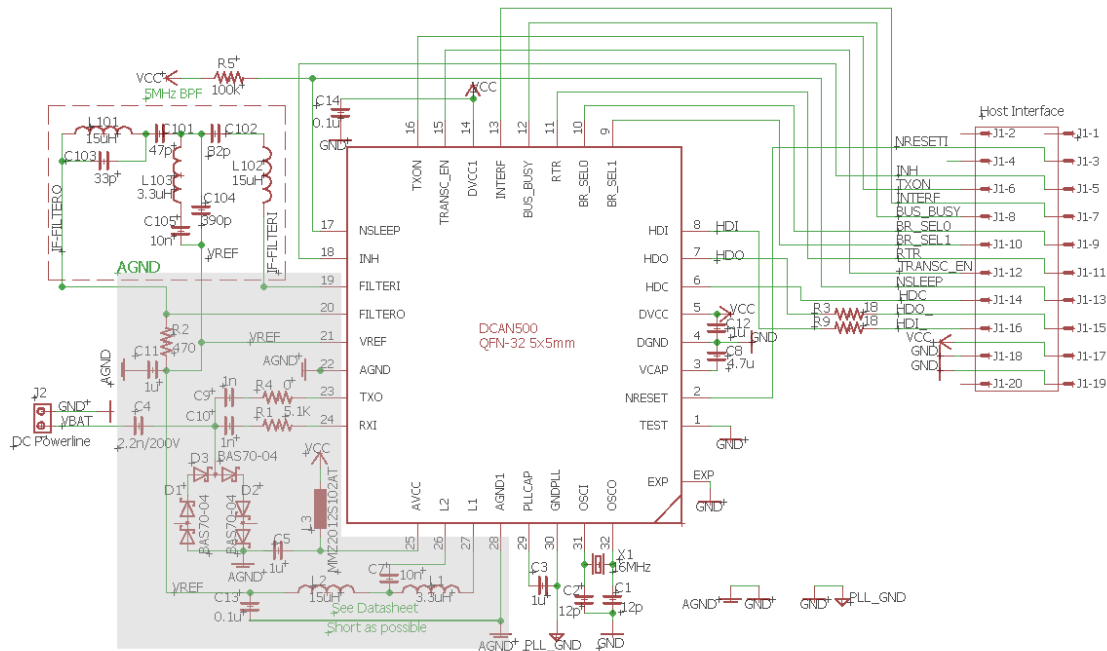
Figure 4- DCAN500 reference schematic

2.5.2   External filter (BPF)

The DCAN500 operates using an external 5MHz band pass filter. The minimum allowable bandwidth of the filters is +/-700 kHz @ 3dB. Narrower bandwidth limits the maximal bitrate.

Figure 5 depicts a recommended 5MHz discrete passive filter.
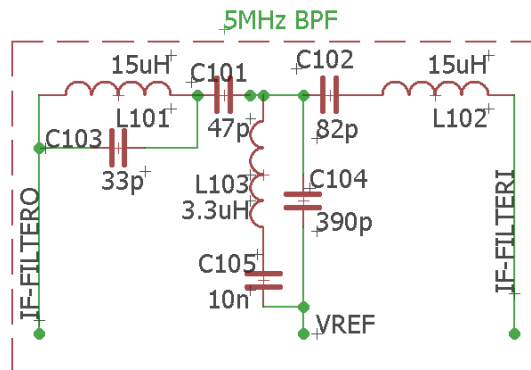
Figure 5 - 5MHz bandpass filter

2.5.3   Crystal oscillator

The device operates with a low cost, small size 16MHz crystal connected between OSCI and OSCO pins. Each of these pins should be connected to the DGND via a load capacitor. The load capacitors values should be determined according to the crystal manufacturer recommendations and the actual PCB layout. The PCB traces should be as short as possible. The overall crystal frequency tolerance should not exceed ± 50ppm.

2.5.3.1 Recommended Crystals

- o **NDK NX2520SA-16MHz SMD, 2.5x2 mm**

- o **NDK NX2016SA-16MHz SMD, 2.0x1.6 mm**

2.5.3.2 16MHz clock from external source

The device can operate from external 16HMz clock source that meets the requirements above.
Figure 6 depicts external 16MHz clock connection to the device.
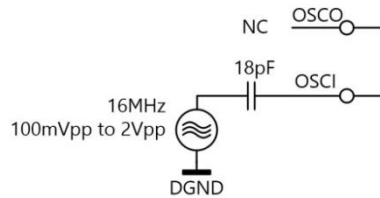
Figure 6 - External 16MHz clock connection

2.5.4 L1 and L2 inductors

The DCAN500 requires one or two inductors for its operation, depending on the desired operating frequency. High Q inductors (above 30) should be selected.

 - For full in-band operation, 5MHz - 30MHz:
  - ➢ L1 - 3.3uH
  - ➢ L2 - 15uH with 1nF series capacitor between L2 pin and L2 inductor.

 - For low in-band operation, 5MHz -12MHz:
  - ➢ L1 - 18uH
  - ➢ L2 - NC

 - For high in-band operation, 12MHz - 30MHz:
  - ➢ L1 - 3.3uH
  - ➢ L2 - NC

Figure 7 depicts in-band operation inductors connection to pins L1 and L2.
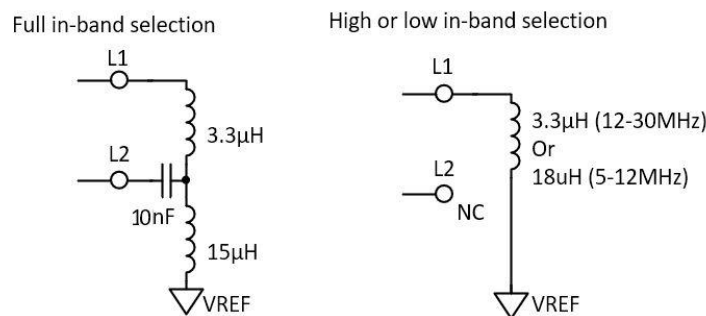
Figure 7 - L1 and L2 inductors connections

2.5.4.1 Recommended L1 & L2 inductors

Table 2 describes recommended L1 and L2 inductors.

Table 2 - Recommended L1 and L2 manufacturers

Inductor	ABRACON	VISHAY	TDK	Coil-Craft
L1=3.3uH	815-AMIL-0805-3R3K-T	ILSB0805ER3R3K	NL453232T-3R3J-PF	1008LS-332XJLC
L2=15uH	815-AMIL-0805-150K-T	ILSB0805ER150K	NL453232T-150J-PF	1008LS-153XJLC
L1=18uH	815-AMIL-0805-180K-T	ILSB0805ER180K	NL453232T-180J-PF	1008LS-183XJLB

2.5.5 Ceramic capacitors

Low ESR capacitors will provide better performance. X5R and X7R capacitors are recommended, especially for Vcap (C8) and PLLCAP (C3).

2.5.6 TXO output level and drive control

The TXO pin output level and drive capability to the powerline is controlled by REG_*1[3]*, as described in Table 3.

Table 3 - TXO signal level

TXON State	REG_1[3]	TX level [V-p-p]
High	'0'	1
	'1' (Default)	2
Low (Rx)		High Z

Setting the TXO output drive capability is made by configuring REG_*1[0]*, as described in Table 4.

Table 4- TXO output drive control

TXON State	REG_1[0]	Output drive [A]	Impedance [Ω]
High	'0' (Default)	33mA	36 [1]
	'1'	66mA	18 [1]
Low (Rx)		Disabled	200k [2]

[1]Series output impedance
[2]Input impedance referenced to VREF

2.5.7 Powerline coupling

The DCAN500 is coupled to the powerline through a single coupling capacitor C$_{coupling}$ that blocks the DC, typically 2.2nF. The capacitor voltage rating depends on the powerline voltage and its expected impulses.
For high voltage powerline applications (e.g. EV battery monitoring system or solar panels), it is required to add proper galvanic isolation.

2.5.8 External protection network

It is recommended to add external diode protection network prior to C$_{coupling}$ to the powerline to protect the device from high powerline impulses (above 2 V-P-P). The protection network consists of three schottky diodes serially connected (for both polarities), with low capacitance (< 10pF) and fast response time (e.g. BAS70-04).

2.5.9 Recommended connection to power-supply

The DCAN500 carrier signal may attenuate strongly due to power-supplies internal filtering capacitors. It is recommended to add an inductor (>22uH) or ferrite bead (>100Ω @ 5MHz-30MHz) in series to the power-supply connection to the DC powerline to avoid carrier signal attenuation.
Figure 8 depicts a typical DCAN500 and its 3.3V power-supply connection to DC powerline.
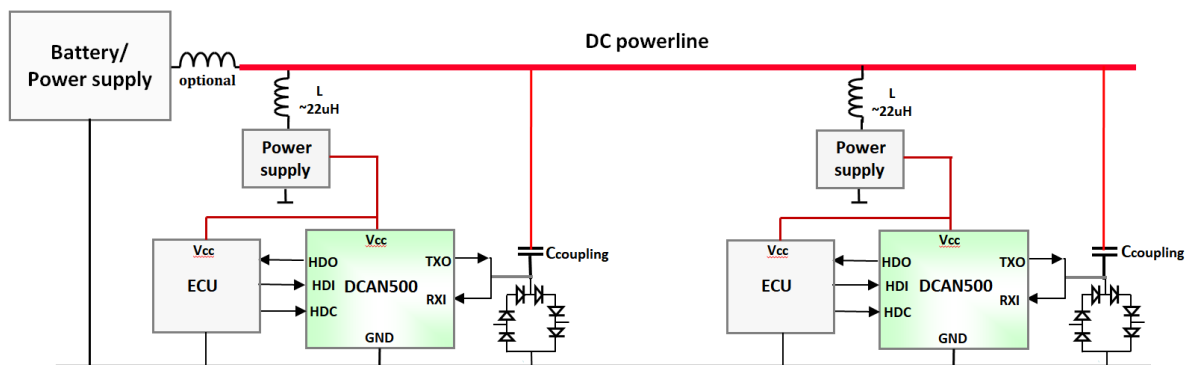
Figure 8– DCAN500 and its 3.3V power-supply connection to powerline.

3. DCAN500 Operation

3.1 Interfacing to CAN ECU

The DCAN500 interfaces directly to a ECU CAN-TX and CAN-RX pins, (3.3V logic) (TRANSC_EN pin must be tied to GND). Optionally, it is possible to interface to traditional CAN-BUS through CANH and CANL signals using external CAN transceiver (TRANSC_EN pin should left floated). However, do not use a mixed network containing both traditional CAN-BUS nodes and DCAN500 nodes.

The CAN communication protocol uses five pins as described in Table 5.

Table 5 - CAN interface pins

HDI	Data Input from the ECU.
HDC	Data/Command select input. When pulled down, the DCAN500 enters command mode, enabling access to DCAN500 control registers.
HDO	Data output to the ECU
RTR	Ready to Receive output (optional feature). Indicating that the device is ready to receive new data bytes from the ECU (i.e. RX-FIFO is not almost full). Used to control the data flow between the ECU and the DCAN500 (see 3.5)
TRANSC_EN	External CAN Transceiver enable pin input. When interfacing a ECU this pin must be tied to GND. HDI is loopback to the HDO. When interfacing a CAN transceiver this pin can be left floated. No loopback between HDO and HDI.

Figure 9 depcits a typical DCAN500 to ECU interfce connection.
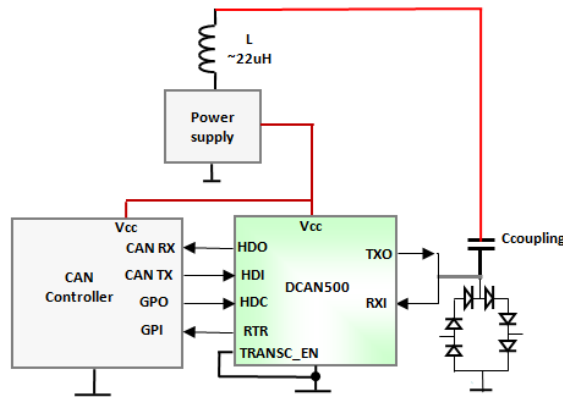
Figure 9 - DCAN500 to ECU interface

Figure 10 depcits DCAN500 to CAN module connection via CAN transceiver.
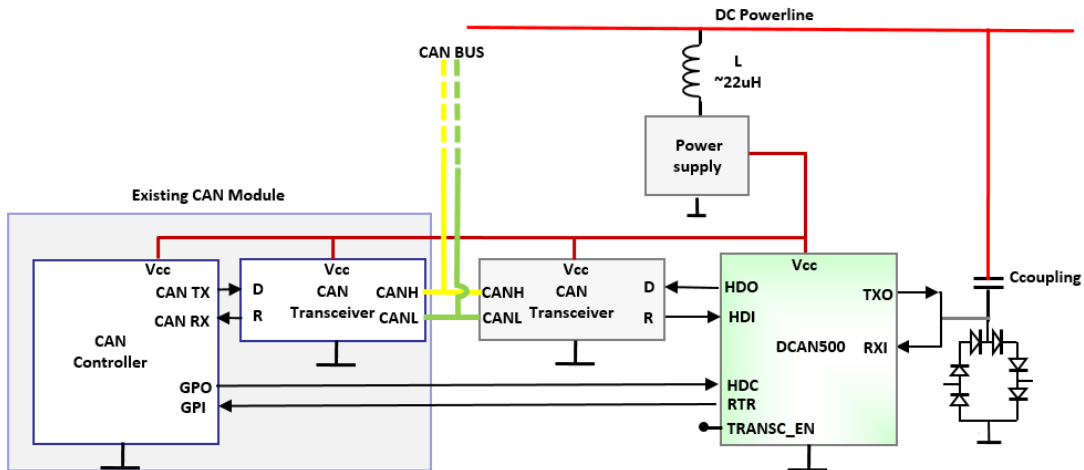
Figure 10 - Optional DCAN500 to ECU interface via CAN transceiver

3.2   DCAN500 Messages

3.2.1   Message structure

The DCAN500 is a powerline CAN gateway device. Each CAN message transferred by the ECU (*CAN-Message*) is constructed into a single DCAN500 CAN frame transmitted over powerline (*CAN-Frame*).

A *CAN-Frame* is constructed from a *Start-frame* consisting of arbitration and preamble patterns followed by packet/s of data bytes (at least 1 packet), and terminated with a *Frame-End,* indicating the last packet of the frame. An Error Correction Code [ECC] protects each data packet.

A *CAN-Frame* may be longer than *CAN-Message*. Therefore, the device has automatic provision ('*DUMMY-MSG'*) to prevent bus contention due to short delay between two CAN messages (see 3.2.2.1).

-    *Start - frame* pattern length: **170 µs minimum**
-    Packet length: **180 µs**

Recommendation: The delay between two consecutive ECU CAN-Messages ≥ 400µs (see Figure 12).
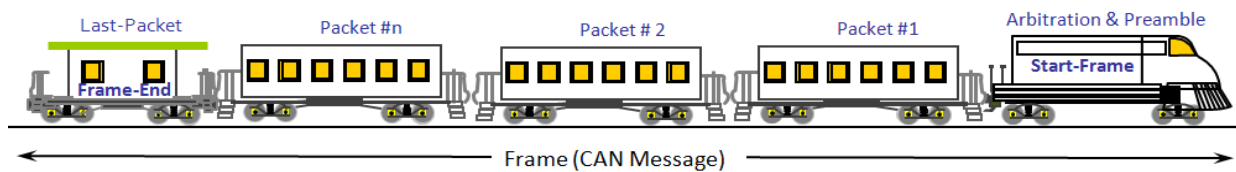
Figure 11 - CAN Frame structure
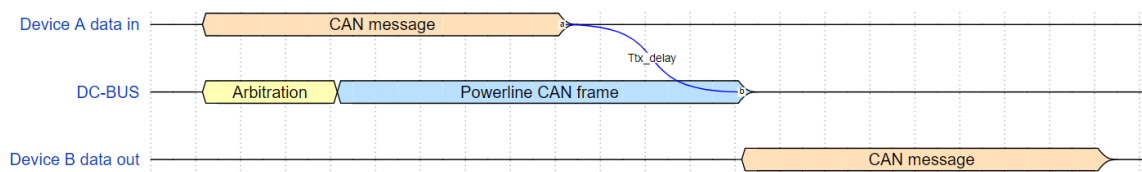
Figure 12 – Typical TX-RX CAN message flow

3.2.2   Transmit flow

Upon receiving a CAN message from its ECU, the device generates *Start-frame* pattern transmission over the powerline. The *Start-frame* consists of unique powerline arbitration based on the ECU's CAN message 11 LSB ID.

When DCAN500 wins the arbitration over the powerline, it will respond to the ECU with ACK at the CAN ACK slot, and transmit a CAN frame to all attached DCAN500 nodes over the powerline.

If DCAN500 loses the arbitration over the powerline due to other device transmission, it will generate a NACK at the ACK slot, abort transmission, receive the *CAN-Frame* from the powerline and transfer it to its ECU.

It is up to the ECU (upper layer) to determine whether to re-transmit the *CAN-Message* or discard it.

3.2.2.1   DCAN500 '*DUMMY-MSG' description* (CAN massage ID zero is preserved)

A *DUMMY-MSG* is a "zero" CAN message, consists of ID = 0, and DLC = 0. Such message always wins the local CAN arbitration with its ECU, generating an artificial delay in the ECU TX flow.

The *DUMMY-MSG* is generated automatically by the DCAN500 to the HDO pin when it detects that the ECU starts a new CAN message transfer while previous CAN message is still being transmitted over the powerline. The ECU loses the arbitration and waits for the duration of the *DUMMY-MSG* and becomes a receiver node without increasing its error counters.

In addition, when the ECU starts a new *CAN-Message* while the DCAN500 is in the middle of CAN frame reception from the powerline, the DCAN500 will also transfer a *DUMMY-MSG*, until completion of powerline *CAN Frame* reception.

To conclude, the DCAN500 will always produce *DUMMY-MSGs* as long as the powerline is not idle while ECU is starting a new CAN message transfer.

Requirement: Avoid using CAN message with ID = 0 as part of CAN messages for DUMMY-MSG proper operation.

ECU may use the DCAN500 pin 12 BUS_BUSY output indication to monitor the powerline BUS activity.

3.2.3   Receive flow

Upon detecting a powerline *CAN-Frame*, the frame is automatically decoded into a *CAN-Message*, inserted to the RX-FIFO and then transferred to ECU via HDO pin.

In case the ECU starts transferring *CAN-Message* while the DCAN500 starts transferring its received powerline *CAN-Frame* to the ECU, a local arbitration between ECU and the DCAN500 begins (same as performed in CAN-BUS). If the ECU wins the local arbitration, the DCAN500 will stop the transfer of the powerline *CAN-Frame* and will get the ECU's CAN message for transmission over the powerline. Then, the DCAN500 will automatically re-transmit the powerline CAN message to its ECU, until successful transfer.

When the ECU loses the local arbitration to the DCAN500, the powerline *CAN-Frame* will be fully transferred to the ECU. Then, ECU may re-transmit its CAN message.

Recommendation: Use the RTR pin to poll the powerline status and pause the ECU's CAN-Message transfer, allowing extraction of the stored CAN-Frame/s from the RX-FIFO (see 3.5).

3.2.4   TX-RX flow examples

3.2.4.1   Example 1 - ECU consecutive *CAN-Messages* transmission

CAN protocol define 3-bit minimal time between two consecutive transmissions. Since the powerline *CAN-Frame* may longer than a ECU's message, therefore the ECU must wait until the powerline is idle.

In this example the DCAN500 issue *DUMMY-MSG* (empty message) to its ECU to delay the transfer of a new message until completion of the ongoing CAN powerline transmission. Figure 13 depicts two CAN messages A and B with a delay less than 400µs. Although CAN message A is still transmitted over the powerline. The ECU starts a new message B. Upon detection of the SOF of the new message B, the DCAN500 immediately initiate a DUMMY-MSG. When the *DUMMY-MSG* completed (ACK by ECU), the powerline is idle again and the ECU re-transmits the *CAN-Message* B by the DCAN500 over the powerline.
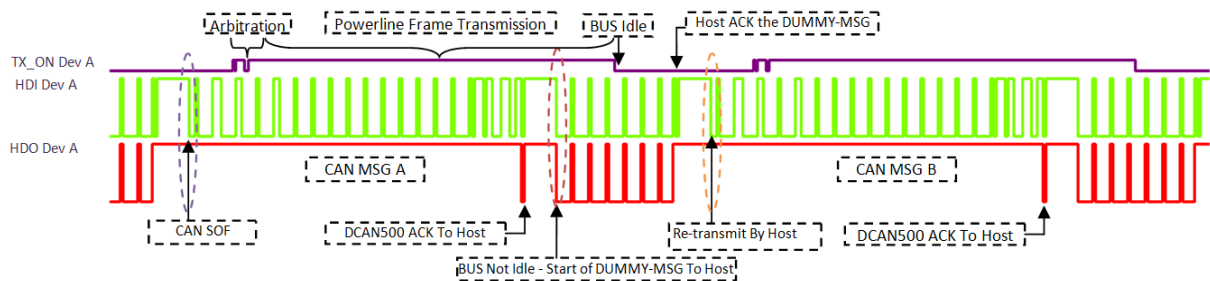
Figure 13 - ECU consecutive CAN message transmission example

Example 2 - ECU generates new SOF while receiving powerline CAN frame from other DCAN500 node.

This case is divided into 2 sub-cases:

Case A -Powerline CAN message was fully decoded and is ready to be transferred to ECU.

In this case, the DCAN500 start transferring the powerline *CAN-Frame* to the ECU.
If the ECU starts at the same time transferring its own *CAN-Message*, a local arbitration will take place between the DCAN500 and the ECU (same as performed in CAN-BUS). The message with the higher ID priority will win.
In case the DCAN500 loses the local arbitration, it will be become a RX station, transmitting the ECU *CAN-Message* over the powerline. Then, the DCAN500 will retransmit its waiting powerline *CAN-Frame* to ECU again.

Case B - Powerline CAN message is detected but not fully decoded before ECU new SOF.

In this case the DCAN500 has detected new powerline *CAN-Frame* prior to start of a new *CAN-Message* from the ECU. The DCAN500 issues a *DUMMY-MSG* until the powerline is idle again. The ECU loses the local arbitration and become a receiver. The DCAN500 repeats to issue *DUMMY-MSG* as long as the powerline is not idle.

Figure 14 depicts an example of Case A and Case B.

The sequence starts when CAN message B is transmitted to the DCAN500 while powerline is Idle. After a while, ECU DEV A tries to transmit its CAN message A. Due to the fact the DCAN500 has already started detecting DEV B's powerline *CAN-Frame*, it will issue *DUMMY-MSG* to DEV A ECU until the powerline is Idle again.
Then, DEV B message is ready to be sent. DCAN500 DEV A will start local arbitration with its ECU. ECU DEV A wins local arbitration and its *CAN-Message* is sent over the powerline. Then, the DCAN500 re-transmit DEV B MSG to its ECU successfully. ECU DEV B receives successfully DEV A CAN MSG.
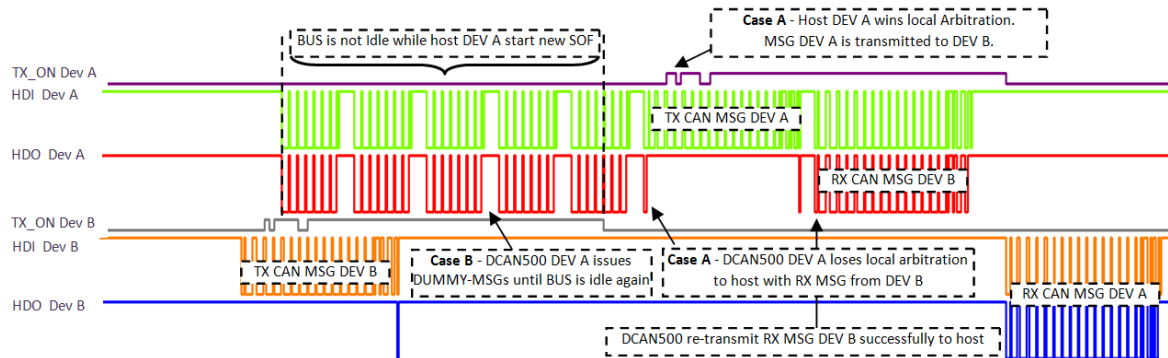
Figure 14 - ECU new SOF while receiving powerline CAN frame from other DCAN500 node example

3.3 Device Configuration

3.3.1 ECU Bitrate selection

The DCAN500 supports CAN A/B bitrates of 83.3kbit/s, 125kbit/s, 250kbit/s, and 500kbit/s.
Requirement: When using bitrate of 500Kbps, CAN message DLC ≥ 3 is required.
Bitrate selection by pins BR_SEL[1:0] as described in Table 6.

Table 6 - CAN bitrate selection

BR_SEL[1:0]	ECU bitrate [kbit/s]
'00'	83.3
'01'	125
'10'	250
'11'	500

The bitrate selection is sampled once after power-up/reset event, and remains until next power-up/reset event.

3.3.2 Carrier frequency configuration

The carrier frequency can be defined between 5MHz to 30MHz with spacing of 100 kHz (Total of 251 selectable carriers). The active carrier frequency selection is made by configuring REG_*2* (see 0). Upon completion of configuration, the DCAN500 will update its operating carrier frequency within 1msec. During this period, the DCAN500 is kept in *Soft-Reset* and will not communicate with its ECU nor detect new *CAN-Frames* from the powerline.

Recommendation: When setting multiple DCAN500 networks to operate over single powerline, select carrier frequencies spaced more than 1.5MHz from each other.
The carrier-selected value is calculated the as given in Equation 1 (3).
Equation 1

$$REG\_2 = (Carrier\ Freq.\ [MHz] - 5) * 10 \tag{1}$$

EXAMPLE 1

❖ When setting the frequency to 14.1MHz:
    REG_2 = (14.1 - 5) * 10 = **0x5B**

EXAMPLE 2

❖ When Setting to 5MHz:
REG_2 = (5 - 5) * 10 = **0x00**

3.4   RX-FIFO handling (optional feature)

The DCAN500 has internal mechanism to buffer between received *CAN-Frames* and its transfer to the ECU. The mechanism contain RX-FIFO with maximal 1024 bytes and RTR interrupt output pin indicating when RX-FIFO is filled up to a configured threshold.

3.4.1   RX-FIFO RTR thresholds configuration

User may define RX-FIFO interrupt (RTR pin) thresholds according to the network expected payload. The interrupt is invoked on RTR pin 11.

The RX- FIFO RTR thresholds control registers is described in Table 7.

Table 7 - RX-FIFOs RTR threshold control

FIFO Threshold Description	Default threshold [Data bytes]	Related Control registers	Comments
RX-FIFO-almost-full[9:0]	256	REG_6[1:0], REG_5[7:0]	Define how many data bytes inserted to RX-FIFO before the interrupt raise. Indicates the ECU to start reading the received frame. See Example 1 in 3.4.1.1

3.4.1.1   Example 1 - *RX-FIFO-almost-full* threshold setting

Configuration *RX-FIFO-almost-full* threshold to 0x384, results in interrupt triggering when there are at least 900 data bytes are stored in Rx-FIFO:
REG_6 = 0x03
REG_5 = 0x84
For more details, please refer the RTR handling in 3.5.

3.4.2   RX-FIFO reset control (Soft-Reset event)

ECU may reset the RX-FIFO stored data by activating a DCAN500 *Soft-reset* event.

A *Soft-reset* is activated while the HDC pin 6 is low.

During *Soft-reset*, the DCAN500 performs only write and read to/from DCAN500 control registers. Neither transmission nor reception to/from the powerline is available. The RX-FIFO is kept in reset.

3.5   RTR pin handling (optional feature)

The Ready to Receive (RTR, pin 11) output allows the ECU to control *CAN-Message* transfers from DCAN500.
When RTR is high, ECU can transfer new *CAN-Message* via HDI pin. When low, ECU should pause its transfer, allowing the DCAN500 to extract stored powerline *CAN-Frames* from the RX-FIFO.
The RTR output state is subject to *RX-FIFO-almost-full* threshold configuration (see Table 7), allowing RX-FIFO overflow protection.
Recommendation: In high payload network, sample the RTR state prior to a new ECU CAN-Message transfer.

3.6   Typical set-up and operation

1. Interface HDI, HDO, HDC, and RTR pins.
2. Set BR_SEL[1:0] pin (see 3.3).
3. Set TRANSC_EN pin according HDI and HDO pins interface (see 3.1).
4. Select a carrier frequency (default 13MHz) (see Section 3.3.2 Carrier frequency configuration).
5. Transmit CAN message via HDI pin to the powerline (with RTR status polling).
6. Receive CAN message from the powerline via HDO pin.

4. Power Operation Modes

The DCAN500 has three power operation modes; Normal, (Sleep) Standby and Sleep.

4.1 Normal mode

In Normal mode, the DCAN500 is either in RX mode, listening for a powerline CAN frame, or in TX mode, transmitting a CAN frame over the powerline.

4.2 Standby mode

The DCAN500 enters Standby mode upon wake-up from Sleep mode, while NSLEEP pin is still low. The DCAN500 is kept in *Soft-Reset*, whereas communication with the ECU is suspended until NSLEEP pin set High.

4.3 Sleep modes (power-saving)

The DCAN500 has four Sleep modes for best power consumption/performance during Sleep. During this mode, only small amount of hardware is operational mainly to detect wake-up messages (*WUM*) from the powerline and returning to Normal mode operation.
Table 8 describes the DCAN500 sleep modes.

Table 8- Sleep modes description

Sleep mode	Description	Power consumption	Performance
Enhanced sleep (SLP1)	The device wakes-up every 32ms to sense the powerline for WUM detection.	Low	Wake-up detection with-in 64mSec. Best in noisy environment.
Fast wake-up (SLP2)	The device continuously monitors the powerline for WUM detection.	Medium	Fast wake-up detection with-in 250uSec.
Very low-power (SLP3)	The device wakes-up every 32ms to sense the powerline for WUM detection.	Very low	Wake-up Detection with-in 64mSec.
Deep Sleep (SLP4)	The device does NOT wake-up to sense for bus activity, staying in deep sleep. Wake-up only locally by the ECU.	Lowest	No bus wake-up detection.

The Sleep modes uses four interface pins as described in Table 9.

Table 9- Sleep interface pins

NSLEEP	Digital input	High - Normal mode is active. Low - Sleep /Standby mode is active.
INH	Digital output	Output indication to Inhibit ECU. High - Normal mode is active. Low - Sleep mode is active.
BUS_BUSY	Digital output	Asserted high while wake-up message is being detected/transmitted over the powerline.
HDC	Digital input	**Normal mode**- ECU Command mode / chip select. **Sleep mode** - ECU wakes-up the DCAN500 locally by toggling the HDC high-low-high. The DCAN500 then exit the Sleep mode to Standby mode (NSLEEP still asserted low), or Normal mode (NSLEEP is high).

4.3.1 Wake-up message (WUM)

When *Auto-WUM* is enabled (REG*[3]*='1'), upon rise of NSLEEP pin, the DCAN500 transmits a broadcast *WUM* over the powerline, to wake-up all network connected devices.
ECU can configure the length of the WUM as described Table 10.

Table 10 - Wake-up message length configuration

REG_3[2]	Wake-up message length
0	*SLP2* - 250usec / *SLP1, SLP3* - 75msec
1	*SLP2* - 1.5msec / *SLP1, SLP3* - 150msec

During WUM transmission, the BUS_BUSY pin is asserted high until WUM transmission is completed, indicating to the ECU the wake-up process status. ECU shall wait for the BUS_BUSY drop, before initiating new bytes transfer.

4.3.2 Entering Sleep mode

During Sleep mode, the device is kept in Soft-reset state and will not transfer data bytes from the ECU nor receive data frames from the powerline. When the device enters Sleep mode, the INH pin is asserted low.
There are two ways to enter Sleep mode;

4.3.2.1 Enter Sleep by NSLEEP

By asserting the NSLEEP pin low, the DCAN500 will enter Sleep mode.

4.3.2.2 Enter Sleep by register setting

By setting REG_*3[7]* high, the DCAN500 will enter Sleep mode, and reset automatically REG_*3[7]* to low.

4.3.3 Exiting Sleep mode

There are three ways to exit Sleep mode. When exiting Sleep mode, the INH pin is raised and the device switches to Standby or Normal mode.

4.3.3.1 Exit Sleep by *WUM* detection

Upon detection of a *WUM*, the device immediately exits Sleep mode, INH pin rises and device enters Standby mode.
In case NSLEEP pin is low, the device remains in Standby mode, where the device is kept in *Soft-reset*.
In case NSLEEP pin is high, the device immediately switches to Normal mode.
During WUM reception, the BUS_BUSY pin is asserted high until WUM reception is completed, indicating the ECU on the wake-up process status. ECU shall wait for BUS_BUSY to drop, before initiating new bytes transfer.

4.3.3.2 Exit sleep by NSLEEP pin

Upon detection of NSLEEP pin rise, the device immediately exits Sleep mode, INH pin rises, and enters Normal mode. When *Auto-WUM* enabled, a WUM is transmitted over the powerline (see 4.3.1).

4.3.3.3 Exit Sleep by toggling HDC

Upon detection of HDC pin toggle high-low-high, the device immediately exits Sleep mode, INH pin rises and enters Standby mode.
In case NSLEEP pin is still low, the device remains in Standby mode, where the device is kept in *Soft-reset*.
In case NSLEEP pin is high, the device immediately switches to Normal mode.
In this case, the WUM will NOT be transmitted over the powerline.
ECU shall use the HDC pin to exit Sleep mode, when the NSLEEP pin is not connected.

4.3.4 Sleep modes description

ECU can select between four Sleep modes (see 5.3).

4.3.4.1 Enhanced Sleep mode (*SLP1*)

By setting REG_*3[1:0]* = '00', the enhanced Sleep mode (*SLP1*) is selected.
When entering*SLP1*, the device wakes-up every 32ms periodically to monitor (sense period) for activity on the powerline. If a WUM is detected, the device exit Sleep modes as described in section 4.3.3.1, otherwise the device return to Sleep mode until next sense period, and so on...

4.3.4.2 Fast wake-up Sleep mode (*SLP2*)

By setting REG_*3[1:0]* = '01', the Fast wake-up Sleep mode (*SLP2*) is selected. The device continuously monitor the powerline for WUM detection. It allows fast WUM detection within 250usec.When WUM is detected, the device exit Sleep mode as described in section 4.3.3.1.

4.3.4.3 Very low-power Sleep mode (*SLP3*)

By setting REG_*3[1:0]* = '10', the Very low-power mode (*SLP3*) is selected. The device wakes-up every 32msec periodically to monitor (sense period) for activity on the powerline. If a WUM is detected, the device exit Sleep modes as described in section 4.3.3.1, otherwise the device return to Sleep mode until next sense period.

4.3.4.4   Deep Sleep mode (*SLP4*)

By setting REG_*3[1:0]* = '11', the Deep Sleep mode (*SLP4*) is selected. The device will NOT wake-up to monitor (sense) the powerline for activity, rather than stay in deep sleep, whereas all its analog resources are shut down to maintain the lowest power consumption.
The device can exit Deep Sleep mode locally only, either by the NSLEEP or by HDC pins (see 4.3.3.2 and 4.3.3.3).

4.3.5   Sleep modes Examples

4.3.5.1   Sleep Example 1 - Enter by NSLEEP, Exit Sleep mode by *NSLEEP & WUM*

Figure 15 depicts entering sleep by NSLEEP and exit sleep by NSLEEP pin (Node A) and WUM detection (Node B).
In this example, the ECU wakes-up device Node A by raising the NSLEEP pin. Upon pull-up the NSLEEP pin, the INH pin is raised and a WUM is transmitted over powerline (*Auto-WUM* is enabled) to wake-up Node B.
While transmitting the WUM, device Node A asserts BUS_BUSY pin high. After completion of WUM transmission, the HDO is raised again (can be used as signal/interrupt to ECU). At Node B side, during its sensing period (e.g. *SLP1),* the WUM is detected, and the INH rises while switching to Standby mode. Node B BUS_BUSY pin is asserted high for the reaming duration of WUM reception. Then, ECU Node B raises the NSLEEP pin, and the device switches to Normal mode.
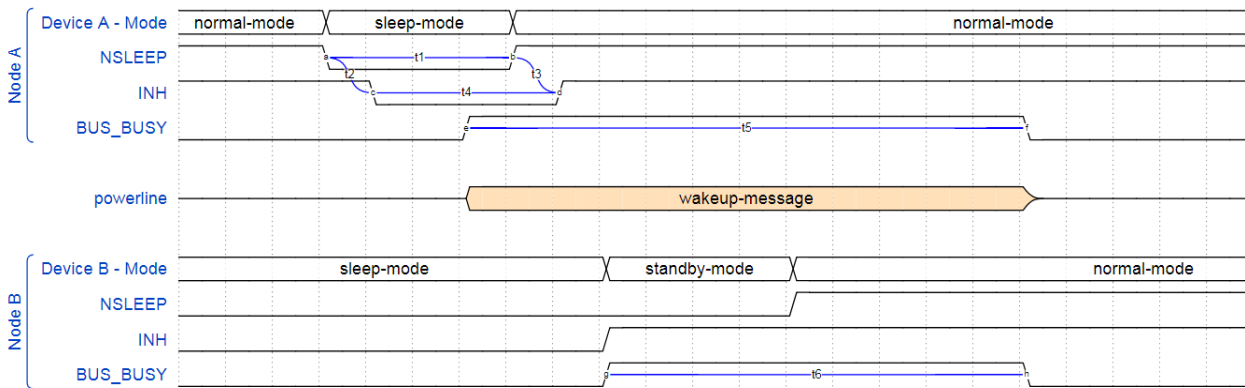
Figure 15 - Enter sleep by NSLEEP, Exit sleep by *NSLEEP& WUM*

4.3.5.2   Sleep Example 2 - Enter sleep by control register bit, exit sleep by HDC

Figure 16 depicts entering sleep by setting REG_*3[7]* high*,* and exiting Sleep mode by toggling the HDC pin.
In this example, ECU configured REG_*3[7]* high using Command mode, the device enters Sleep mode and INH pin drops. After a while, ECU toggle HDC pin low to high, and the device exits Sleep mode without transmitting the WUM, raising the INH pin and switching to Normal mode again.
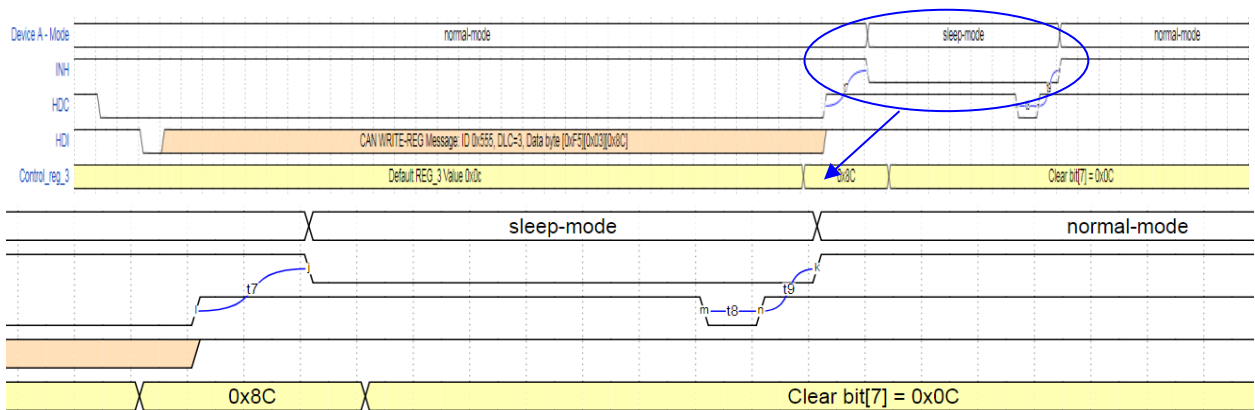
Figure 16 - Enter sleep by control register bit, Exit sleep by *HDC*

5. DCAN500 Registers

The DCAN500 contains internal registers for configuration and status check. Each of these registers is accessible by the ECU for *Read* and *Write* operations. The access method to these registers is described in section 5.6. This section elaborates on the registers and their default values after power-up/reset.

Table 11 - Registers summary table

Register name	Addr.	Description
REG_1 - 'Device Control 1'	0x01	Transmit level control
REG_2 - 'Frequency Select'	0x02	Carrier frequency selection
REG_3 - 'Sleep & IO Control'	0x03	Sleep modes and IO pins
REG_5 - 'RX-FIFO Threshold 1'	0x05	*RX-FIFO-almost-full* threshold lower nibble
REG_6 -'RX-FIFO Threshold 2', *Rx-FIFO overflow* indication	0x06	*RX-FIFO-almost-full* threshold higher nibble, *Rx-FIFO overflow* error indication.

5.1 REG_1 - 'Device Control 1' (Address 0x01)

| Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[1]	[1]	[1]	[1]	R/W [1]	[0]	[0]	R/W [0]
1	1	1	1	TX signal level	0	0	Enable TXO high power

Bit [0]   - Enable TXO high power. Set this bit to enable maximal TXO drive of 66mA, clear this bit for maximal TXO drive of 33mA (see section 2.5.6).
Bit [1]   - '0'
Bit [2]   - '0'
Bit [3]   - TX signal level control at TXO pin: '0' - 1Vpp, '1'- 2Vpp (see section2.5.6).
Bit [7:4]   - '1111'
R - Readable bit,   W - Writeable bit   [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.2 REG_2 - 'Frequency Select' (Address 0x02)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
Carrier Frequency Configuration							

Bits [7:0]   - Carrier Frequency configuration for in-band operation. Default configuration is 13MHz
(See section 3.3.2 - 3.3.2Carrier frequency configuration).

5.3 REG_3 - 'Sleep & IO Control' (Address 0x03)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W [0]	[0]	[1]	[0]	R/W [1]	R/W [1]	R/W [0]	R/W [0]
Enter Sleep mode	0	1	0	Auto WUM	Long WUM	Sleep modes selection	

Bit [1:0]   - '00' - Enhanced Sleep mode [*SLP1*], '01' -Fast wake-up Sleep mode[*SLP2*], '10' - Very low-power sleep mode [*SLP3*], '11' - Deep Sleep mode [*SLP4*] (see section4.3).
Bit [2]   - Control powerline wake-up message duration (see Table 10).
Bit [3]   -Auto wake-up message (WUM): '0' disables transmission of WUM after wakeup from NSLEEP pin.
Bit [4]   - '0'
Bit [5]   - '1'
Bit [6]   - '0'
Bit [7]   -Enter Sleep mode reg. Instead of entering Sleep mode through the NSLEEP pin, user can activate the Sleep mode selected in bits[1:0], by setting bit[7]. After entering Sleep mode, bit[7] is automatically cleared to '0'.
R - Readable bit,   W - Writeable bit   [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.4 REG_5 - 'RX-FIFO Almost full Threshold 1' (Address 0x05)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

W/R[0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
RX-FIFO-almost-full[7:0] *threshold*							

Bits [7:0]   - *RX-FIFO-almost-full* [7:0], eight LSB of *RX-FIFO-almost-full*[9:0] threshold bits[9:8] are configured in REG_6[1:0].

RX-FIFO-almost-full[9:0] threshold - default set to 256 data bytes

5.5   REG_6 - RX-FIFO Almost full Threshold 2' and overflow indication (Address 0x06)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
[0]	[0]	R	[0]	[0]	[0]	R/W [0]	R/W [1]
0	0	*Rx-FIFO* overflow	0	0	0	*Rx-FIFO-almost-full[9:8] threshold*	

Bits [1:0] -   *RX-FIFO-almost-full*[9:8],*Two MSB of RX-FIFO-almost-full*[9:0] threshold.
Bits [4:2] -   '000'.
Bits [5]   -   Read only - *Rx-FIFO* overflow error indication.
Bits [7:6] -   '00'.
R - Readable bit,   W - Writeable bit   [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.6   Registers configuration (Command mode)

The Command mode allows the ECU to access the DCAN500 internal registers for write and read operations. Controlling these registers is done by lowering HDC pin and sending a pre-defined CAN-Message to the registers as described below. During Command mode, the DCAN500 is in *Soft-Reset* state, RX-FIFO is reset and all data in the FIFO is erased and the device cannot send or receive message to/from the powerline.

5.6.1   WRITE-REG command

A Write-REG command is constructed from CAN A message, with ID = 0x555 and DLC = 3, as described in Table 12.

Table 12 - WRITE-REG command structure

1st data Byte	2nd data Byte	3rd data Byte
0xF5	Control register address	Data to write

The 1st CAN data byte is the write command byte.

The 2nd CAN data byte is the designated control register address to write to.

The 3rd CAN data byte is the data byte value to write.

The new configured value is kept until the next power-up/reset event.

For example, writing 0x34 to REG_2 (address 0x02) preformed as follows (depicted in Figure 17):

1. Lower the HDC pin (Enter Command mode).

2. Wait at least 100nsec

3. Transfer CAN A message with ID = 0x555 and 3 data bytes: [0xF5][0x02][0x34]

4. The value 0x34 is written to REG_2.

5. Wait at least 100ns.

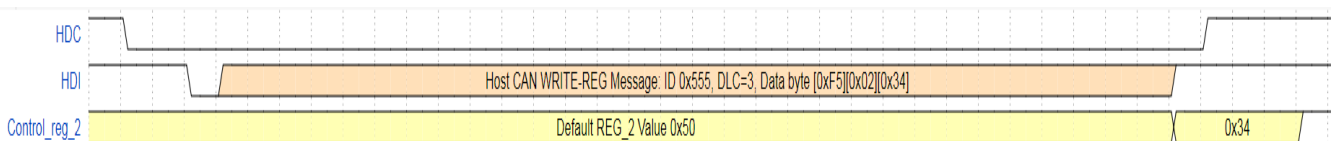6. Raise the HDC pin (Exit Command mode to Normal mode).

Figure 17 - WRITE-REG example

5.6.2   READ-REG command

A READ-REG command is constructed from as CAN A message, with ID = 0x555 and DLC = 2 as described in Table 13.

Table 13 - READ-REG command structure

1st data Byte	2nd data Byte
0xFD	Control register address

1st CAN data byte is the Read command byte.

2nd CAN data byte is the designated register address to read from.

Upon receiving a complete READ-REG CAN message, the DCAN500 will response with a feedback CAN message with ID 0x00, and DLC =1, consists of the read register value.

For example, reading from REG_3 (address 0x03) is performed as follows (depicted in Figure 18).

1. Lower the HDC pin (Enter Command mode).

2. Wait at least 100nsec

3. Transfer CAN A message with ID = 0x555 and 2 bytes: [0xFD][0x03]

4. Wait for the DCAN500 response CAN A message with ID=0x000, and one data byte that holds the value of REG_3.

5. Wait at least 100ns.

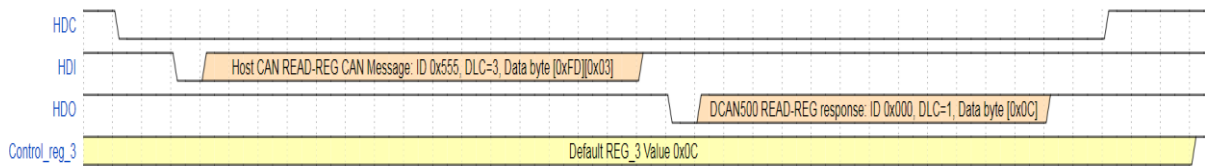6. Raise the HDC pin (Exit Command mode to Normal mode).

Figure 18 - READ-REG example

6. Specifications

Table 14 - Absolute maximal rating

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Input voltage, DC	V_{im}		-0.6	3.3	3.9	V
Output voltage, DC	V_{om}		-0.6	3.3	3.9	V
Ambient temperature	T_{am}		-40		125	°C
Storage temperature	T_{sm}		-55		150	°C

Table 15 - Recommended operation conditions

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DVCC} V_{AVCC}		3.0	3.3	3.6	V
Supply Voltage ripple	V_{CC_RIP} A_{VCC_RIP}	Max 2.5MHz, waveform type of triangular		50m		V-p-p
Ambient operating temperature range	T_A		-40		105	°C
Minimum high level input voltage	V_{IH}		2			V
Maximum low level input voltage	V_{IL}				0.8	V
Minimum high level output voltage	V_{OH}		2.4			V
Maximum low level output voltage	V_{OL}				0.4	V
Maximal output current	I_{out}	see Table 1				
Maximum input current	I_{IN}		-1		1	µA

Table 16 - Device characteristics

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Extrnal componenets requierments						
Powerline coupling capacitor	$C_{coupling}$	Capacitor rate should be selected with respect to powerline voltage		2.2		nF
Protection diodes capacitance	D_{protec}			10		pF
Capacitor at VCAP	V_{cap}		1	4.7		µF
Capacitor at PLLCAP	PLL_{cap}		1			µF
Capacitor at VREF	$VREF_{cap}$		1			µF
Inductor at L1	L1	see 2.5.4		3.3 / 18		µH
Inductor at L2	L2			15		µH
L1 pin input capacitance					1	pF
Crystal frequency	$Xtal_{freq}$	see2.5.3		16		MHz
Crystal frequency tolerance	$Xtal_{ppm}$				50	±ppm
AC signals characterics						
Tx signal at TXO	TXO_{lev}	TXON high (transmission is active) see 2.5.6	1		2	V-p-p
TXO input impendace	TXO_{In}	TXON low (transmission is not active)	200k			Ω
TXO output impedance	TXO_{out}	TXON high (transmission is active)	18		36	Ω
TXO driving strength	I_{TXO}	TXON high (transmission is active)	33		66	mA
Rx signal at RXI	RXI_{lev}		10m		3.3	V-p-p
RXI input impedance	RXI_{In}		5.1k			Ω
Carrier Frequency in-band (channels selection)	F_c	Selectionresolutionis 100kHz, total of 251 carrier frequencies,	5		30	MHz

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
		see 3.3.2				
Adjucent channels spacing	F_{adj}	The space between two adjucent channels operating over same powerline.	1.5			MHz
Timing requierments of CAN interface						
CAN bitrate	CAN_{br}	ECU CAN bitrate. see Table 6.	83.3		500 [1]	kbit/s
ECU TX delay	T_{tx_delay}	The minimal delay between two consecutive ECU CAN messages. see 3.2.2.1.	400			µs
RX-FIFO size		see 3.4			1024	Byte
Timing of device operation modes						
Power-cycle/ hard-reset	T_{init}	Initialzation time after power-cycle or hard-reset event.		2		ms
Carrier frequency setting	T_{freq_cng}	Carreri frequnecy change process time		1		ms
Current Consumtption @ 3.3V						
Normal TX mode	I_{Tx}	TXON high (transmission is active)		82		mA
Normal RX mode	I_{RX}	TXON low (transmission is not active)		48		mA

1 CAN message DLC ≥ 3 is required.

7. DCAN500 PCB layout recommendation

Figure 19 below are examples of two layer PCB layout. Separate analog ground is surrounding the analog parts of the design.
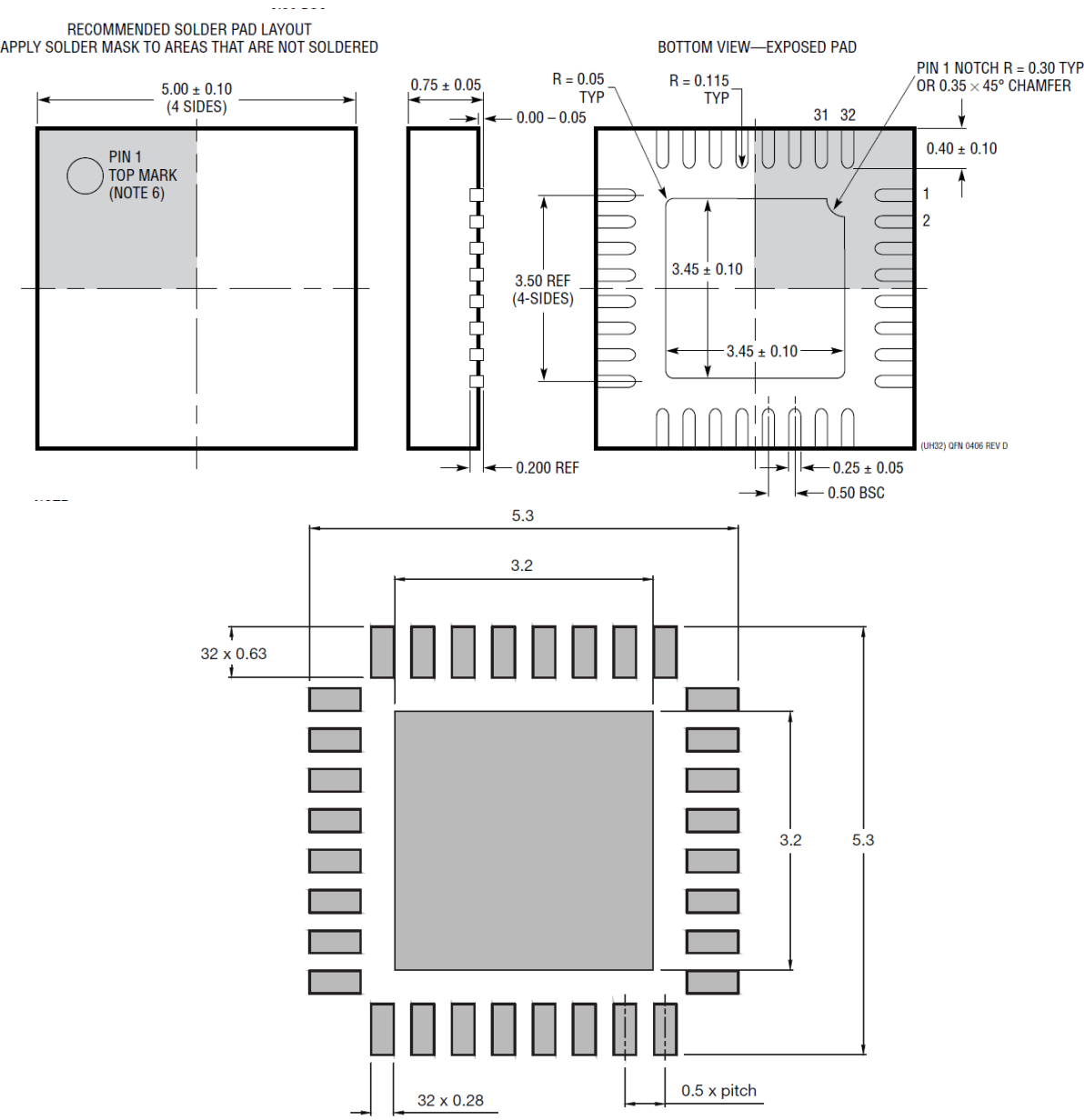

Figure 19 – Grounds layout reference

- ✓ Analog ground layer and GND PLL should be connected to the digital ground near the Expose pad.
- ✓ VCC and DGND layout traces should be as wide as possible. Connect a 0.1uF capacitor between each VCC and DGND pins, as close as possible to the pins.
- ✓ It is recommended to keep the traces connecting the 3.3V power supply to VCC pins as short as possible with wide PCB traces.
- ✓ Connect L1, L2, C3, C5, C7, C8, C11, and C12 as close as possible to their pins.
- ✓ Connect R1 as close as possible to RXI pin.
- ✓ Connect all filtering caps as close as possible to their pins.
- ✓ Connect crystal and its capacitors close to OSCI and OSCO pins. Keep DGND plan around them.

8.   Package, Mechanical

The device package is QFN 32 5mm x 5mm

8.1   Mechanical Drawing

RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD

5.00 ± 0.10
(4 SIDES)

PIN 1
TOP MARK
(NOTE 6)

0.75 ± 0.05

0.00 – 0.05

R = 0.05
TYP

R = 0.115
TYP

PIN 1 NOTCH R = 0.30 TYP
OR 0.35 × 45° CHAMFER

31   32

0.40 ± 0.10

1
2

3.50 REF
(4-SIDES)

3.45 ± 0.10

3.45 ± 0.10

0.200 REF

0.25 ± 0.05

0.50 BSC

(UH32) QFN 0406 REV D

5.3

3.2

32 x 0.63

3.2

5.3

32 x 0.28

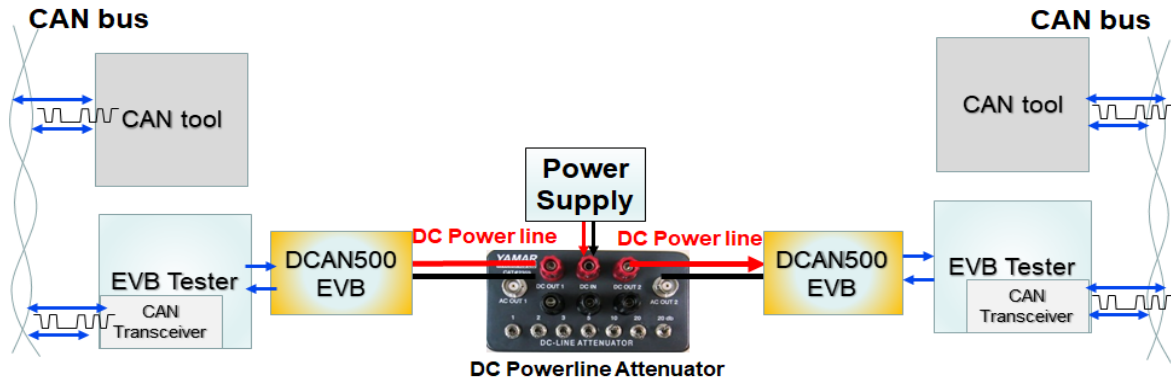0.5 x pitch

9.   Test Environment

Figure 20 depicts the DC-BUS Test environment that allows testing the DCAN500 devices in emulated lab DC powerline environment.
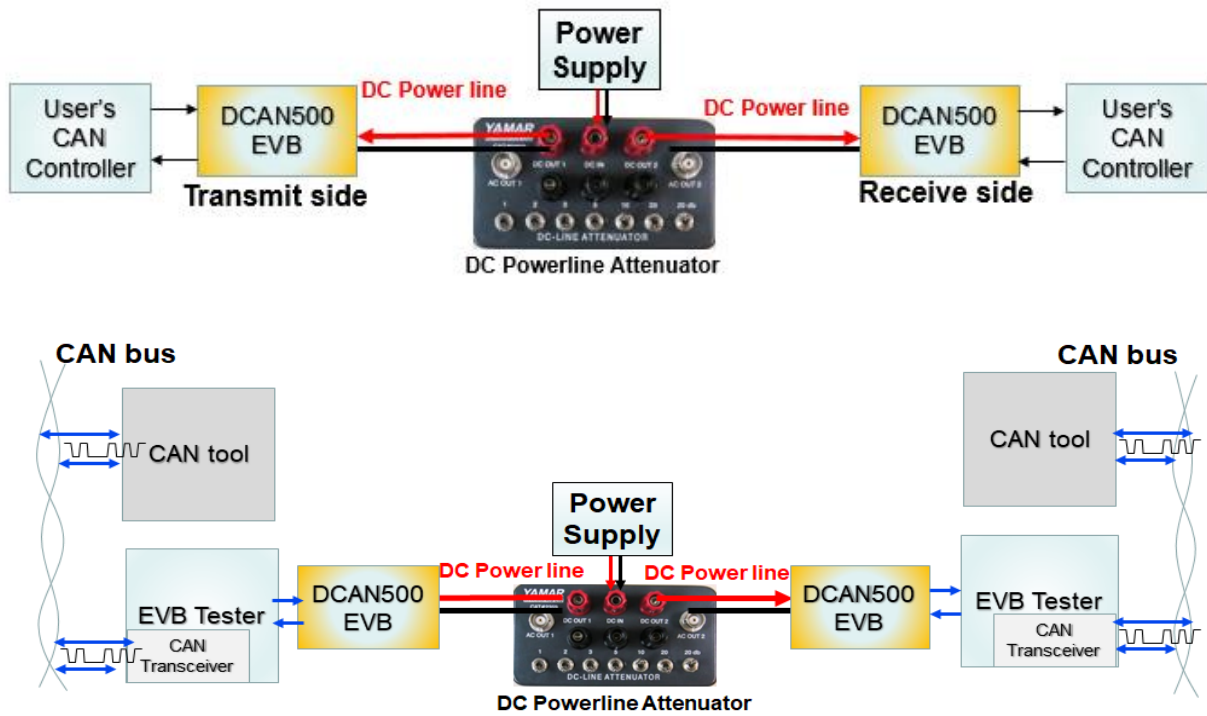

Figure 20 - DC-BUS Test environment

This test environment consists of two DCAN500 evaluation boards (EVB), two EVB Tester boards (optional), DC powerline Attenuator (optional) and user's ECUs.

User can interface directly from a CAN controller with the DCAN500. At the transmitting side, the ECU generates CAN test messages. At the receiver side, the DCAN500 EVB receives the test message, transfer it to the other ECU and analyze the received messages for errors.

Adding the two EVB Tester boards, allows also stand-alone mode (auto TX-RX test), on-board DCAN500 configuration switches and on-board CAN transceiver which can interface to an existence CAN BUS.

See EVB Tester board manual for more details.

The DC-powerline attenuator is used to test the communication in variable attenuation levels (0-61dB), emulating a DC powerline environment. When powering the ECU directly to the powerline, it is recommended to add an inductor (> 22uH) in serial to its power supply to avoid strong attenuation due to the power supply input filtering capacitors.

Revision History

Rev.	Date	Description
0.72	10/05/2019	Initial preliminary revision.
0.73	22/7/2019	Updated 5MHz filter.
0.74	2/8/2019	Rearrange paragraphs.
0.75	05/09/2019	Update schematic, Table 16.
0.76	23/09/2019	Editing.
0.77	02/10/2019	Update Table 2 and Figure 7.
0.78	14/11/2019	Update Figure 4 and NSLEEP pin description.

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