Highly Versatile Buck-Boost Ambient Energy Manager with Source Voltage Level Configuration

Feature

Ultra-low power start-up

- Cold start from 275 mV input voltage and 3 µW input power (typical)

Constant input voltage regulation

- Optimized for intermittent and pulse power
- Selectable operating input voltage from 140 mV to 4.5 V

Adaptive and smart energy management

- Switches automatically between boost, buck-boost and buck operation, to maximize energy transfer from its input to the output
- Automatically selects between the source, storage element
- Automatically select the output between the internal supply, the load and the storage element

Load supply voltage

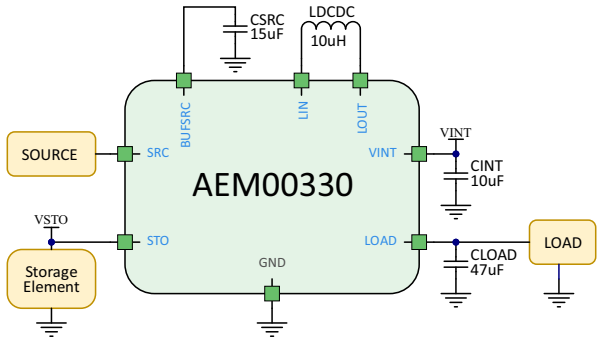
- Current drive capability: 30 mA in low power mode, 60 mA in high power mode
- Selectable load voltage from 1.2 V to 3.3 V

Battery protection features

- Selectable over-charge and over-discharge protection for any type of rechargeable battery or (super-)capacitor
- Fast super-capacitor charging
- Dual cell super-capacitor balancing circuit

Smallest footprint, smallest BOM

- Only four external components are required
- One 10 µH inductor
- Three capacitors: one 10 µF, one 15 µF, one at least 47 µF



Description

The AEM00330 is an integrated energy management circuit that extracts DC power from an ambient energy harvesting source to simultaneously supply an application and store energy in a storage element. The AEM00330 allows to extend battery lifetime and ultimately eliminates the primary energy storage element in a large range of applications.

Two different storage elements can be connected: one for storing energy and another one for coupling the load output voltage. At start-up, user can choose to charge the storage element first or the load capacitor first.

Thanks to its selectable operating input voltage, it is possible to set a voltage at which the AEM00330 operates. This voltage is between 140 mV and 4.5 V.

With its unique cold start circuit, the AEM00330 can start harvesting with an input voltage as low as 275 mV and from an input power of 3 µW. The preset protection levels determine the storage element voltages protection thresholds to avoid over-charging and over-discharging the storage element and thus avoiding damaging it. Those are set through configuration pins. Moreover, special modes can be obtained at the expense of a few configuration resistors.

The load voltage can be selected to cover most application needs, with a maximum available load current of 60 mA.

Applications

- Door access systems
- Smart wearable sensors
- Smart switches home/building
- Point-of-sales (POS)

Device Information

Part Number	Package	Body size [mm]
10AEM00330J0000	QFN 40-pin	5x5mm

Evaluation Board

Part Number
2AAEM00330J001

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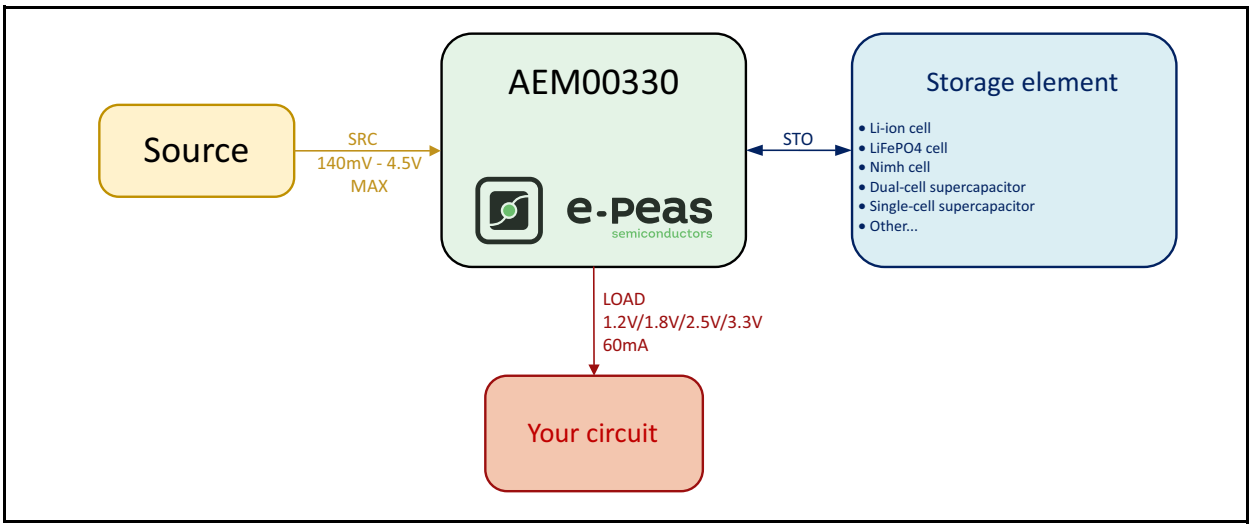

Figure 1: Simplified Schematic View

1. Introduction

The AEM00330 is a full-featured energy efficient power management circuit able to harvest energy from an energy source (connected to SRC) to supply an application circuit (connected to LOAD) and use any excess of energy to charge a storage element (connected to STO). This is done with a minimal bill of material: only 3 capacitors and one inductor are needed for a basic setup.

The heart of the AEM00330 is a regulated switching DCDC converter with high power conversion efficiency.

At first start-up, as soon as a required cold-start voltage of 275 mV and a sparse amount of power of at least 3 µW is available at the source, the AEM00330 coldstarts. After the cold start, the AEM extracts the power available from the source if the working input voltage is higher than $V_{SRC,REG}$.

Through four configuration pins (STO_CFG[3:0]), the user can select a specific operating mode out of 15 modes that cover most application requirements without any dedicated external component. Those operating modes define the protection levels of the storage element. If none of those 15 modes fit the user's storage element, a custom mode is also available to allow the user to define a mode with custom specifications.

Status pins ST_STO, ST_STO_RDY and ST_STO_OVDIS provide information about the voltage levels of the storage element. ST_STO is asserted when the voltage of the storage element V_{STO} is above V_{CHRDY} and is reset when the voltage drops below V_{OVDIS}. ST_STO_RDY is asserted when V_{STO} is above V_{CHRDY}, and reset when V_{STO} drops below V_{CHRDY}. ST_STO_OVDIS is asserted when V_{STO} drops below V_{OVDIS} and reset when V_{STO} is above V_{OVDIS}. Status pin ST_LOAD is asserted when the load voltage V_{LOAD} rises above $V_{LOAD,TYP}$, and is reset when V_{LOAD} drops below $V_{LOAD,MIN}$.

Depending on the harvester and the application, the source regulation voltage, $V_{SRC,REG}$, can be configured thanks to six configuration pins (SRC_LVL_CFG[5:0]).

Once started, if at any time the load requires more power than can be harvested from the energy source, the AEM00330 automatically uses the storage element to keep the load supplied.

The AEM00330's DCDC converter can work in two modes: LOW POWER MODE and HIGH POWER MODE, each one of these being optimized for a power range on SRC and LOAD.

The charging of the storage element can be prevented by pulling EN_STO_CH to GND, typically to protect the storage element if the temperature is too low/high to safely charge it.

The AEM00330 also implements a SLEEP STATE, which reduces the quiescent current to avoid wasting the energy stored on the storage element when EN_SLEEP is asserted.

At start-up, user can choose to prioritize starting the application circuit connected on LOAD, or charging the storage element connected on STO. This is set by the STO_PRIO pin.

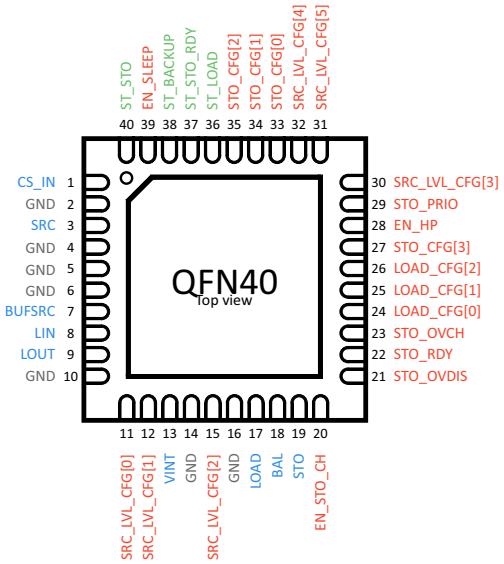

Figure 2: Pinout Diagram QFN 40-pin

NAME	PIN NUMBER	FUNCTION
Power pins		
CS_IN	1	Input for the external cold start circuit.
SRC	3	Connection to the harvested energy source.
BUFSRC	7	Connection to an external capacitor buffering the DCDC converter input.
LIN	8	DCDC inductance connection.
LOUT	9	DCDC inductance connection.
VINT	13	Internal voltage supply. On QFN48 package, both pins must be tied together.
LOAD	17	Output voltage to supply the load.
STO	19	Connection to the energy storage element - battery or (super-)capacitor. Cannot be left floating. Must be connected to a minimum capacitance of 100 µF or to a rechargeable battery. On QFN48 package, both pins must be tied together.
BAL	18	Connection to mid-point of a dual-cell supercapacitor (optional). Must be connected to GND if not used.
Status pins		
ST_STO	40	Logic output. Asserted when the storage device voltage V_{STO} rises above the V_{CHRDY} threshold, reset when V_{STO} drops below the V_{OVDIS} threshold. High level is V_{STO}.
ST_LOAD	36	Logic output. Asserted when the LOAD voltage V_{LOAD} rises above the $V_{LOAD,TYP}$ threshold. Reset when V_{LOAD} drops below $V_{LOAD,MIN}$ threshold. High level is V_{LOAD}.
ST_STO_RDY	37	Logic output. Asserted when V_{STO} is above V_{CHRDY}, reset when V_{STO} drops below V_{CHRDY}. High level is V_{LOAD}.
ST_STO_OVDIS	38	Logic output. Asserted when the AEM00330 state is SHUTDOWN STATE or PRIMARY BATTERY STATE, reset when in any other state. High level is V_{LOAD}.

Table 1: Power and Status Pins

NAME	PIN NUMBER	Function
Configuration pins		
SRC_LVL_CFG[0]	11	Used for the configuration of the source voltage level.
SRC_LVL_CFG[1]	12	
SRC_LVL_CFG[2]	15	
SRC_LVL_CFG[3]	30	
SRC_LVL_CFG[4]	32	
SRC_LVL_CFG[5]	31	
LOAD_CFG[0]	24	Used for the configuration of LOAD output voltage V_{LOAD}.
LOAD_CFG[1]	25	
LOAD_CFG[2]	26	
STO_CFG[0]	33	Used for the configuration of the threshold voltages for the energy storage element (V_{OVDIS}, V_{CHRDY} and V_{OVCH}).
STO_CFG[1]	34	
STO_CFG[2]	35	
STO_CFG[3]	27	
STO_PRIO	29	- Pulled up to VINT: storage device (STO) has highest priority at start-up - Pulled down to GND: load (LOAD) has highest priority at start-up
STO_OVCH	23	Used for the configuration of the threshold voltages (V_{OVDIS}, V_{CHRDY} and V_{OVCH}) for the energy storage element when STO_CFG[3:0] are set to custom mode (optional). Must be left floating if not used.
STO_OVDIS	21	
STO_RDY	22	
EN_SLEEP	39	- Pulled up to LOAD: SLEEP STATE enabled - Pulled down to GND: SLEEP STATE disabled
EN_STO_CH	20	- Pulled up to LOAD: enables the charging of the battery - Pulled down to GND: disables the charging of the battery
EN_HP	28	- Pulled up to VINT: HIGH POWER MODE enabled - Pulled down to GND: HIGH POWER MODE disabled
Other		
GND	2, 4, 5, 6, 10, 14, 16	Ground connection, best possible connection to PCB ground plane.
	Exposed pad	

Table 2: Configuration and Ground Pins

2. Absolute Maximum Ratings

Parameter	Value
Voltage on LOAD, STO, SRC, BUFSRC, LIN, LOUT, BAL, CS_IN, EN_SLEEP, EN_STO_CH	-0.3 V to 5.5 V
Voltage on VINT, SRC_LVL_CFG[5:0], LOAD_CFG[2:0], STO_CFG[3:0], STO_PRIO, STO_OVCH, STO_OVDIS, STO_RDY, EN_HP	-0.3 V to 2.75 V
Operating junction temperature	-40 °C to 125 °C
Storage temperature	-65 °C to 150 °C
ESD HBM voltage	> 2000 V
ESD CDM voltage	> 500 V

Table 3: Absolute Maximum Ratings

3. Thermal Resistance

Package	θJA	θJC	Unit
QFN 40-pin	TBD	TBD	°C/W

Table 4: Thermal Resistance

ESD CAUTION	
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper EESD precautions should be taken to avoid performance degradation or loss of functionality

Table 5: ESD Caution

4. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power Conversion						
$P_{SRC,CS}$	Source power required for cold start	V_{STO} > Vchrdy		3		µW
		V_{STO} < Vchrdy		6		µW
V_{SRC}	Input voltage of the energy source	During cold start		0.275	4.5	V
		After cold start	0.14		4.5	V
$V_{SRC,REG}V_{SRC,REG}$	Regulation voltage of the source	See Table 11	Depends on SRC_LVL_CFG[5:0] configuration			V
Storage element						
V_{OVCH}	Maximum voltage accepted on the storage element before disabling its charging	see Table 9	Depends on STO_CFG[3:0] configuration			V
V_{CHRDY}	Minimum voltage required on the storage element before asserting the ST_STO					V
V_{OVDIS}	Minimum voltage accepted on the storage element before entering into SHUTDOWN STATE					V
Load Output Voltage						
$I_{LOAD,MAX}$	LOAD current drive capability	V_{LOAD} = 1.8V V_{STO} > 1.6V HP_EN = 1		60		mA
		V_{LOAD} = 2.5V V_{STO} > 1.6V HP_EN = 1		60		
		V_{LOAD} = 3.3V V_{STO} > 1.8V HP_EN = 1		60		
V_{LOAD}	Output voltage	see Table 10	Depends on LOAD_CFG[2:0] configuration			V
Internal supply & Quiescent Current						
V_{VINT}	Internal voltage supply			2.2		V
I_Q	Quiescent current on STO	V_{STO} = 3.7V V_{LOAD} = 2.5V EN_SLEEP = 0 HP_EN = 0		875		nA
Symbol	**Logic Level**		**Low**		**High**	
Logic output pins						
ST_STO	Logic output levels on the status STO pin		GND		V_{STO}	
ST_LOAD	Logic output levels on the status LOAD pin		GND		V_{LOAD}	
ST_STO_RDY	Logic output levels on the status STO_READY pin		GND		V_{LOAD}	
ST_STO_OVDIS	Logic output levels on the status STO_OVDIS pin		GND		V_{LOAD}	

Table 6: Typical Electrical Characteristics

5. Recommended Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
External Components					
LDCDC	Inductor of the DCDC converter		10		µH
CSRC	Capacitor decoupling the SRC terminal	15			µF
CINT	Capacitor decoupling the VINT terminal	10			µF
CLOAD	Capacitor decoupling the LOAD terminal	40			µF
CSTO	Optional - Capacitor on STO if no storage element is connected (see Section 8.7.1)	100			µF
STO_OVCH	Configuration of V_{OVCH} in custom mode	1	Section 8.4	100	MΩ
STO_OVDIS	Configuration of V_{OVDIS} in custom mode				
STO_RDY	Configuration of V_{CHRDY} in custom mode				
Symbol	Logic Level	Low		High	
Logic input pins					
LOAD_CFG[2:0]	Configuration pins for the LOAD voltage	GND		VINT	
SRC_LVL_CFG[5:0]	Configuration pins for the SRC voltage level	GND		VINT	
STO_CFG[3:0]	Configuration pins for the STO voltage	GND		VINT	
STO_PRIO	Configuration pin for the controller	GND		VINT	
EN_STO_FT	Configuration pin for the controller	GND		VINT	
EN_SLEEP	Configuration pin for the controller	GND		LOAD	
EN_STO_CH	Configuration pin for the controller	GND		LOAD	
EN_HP	Configuration pin for the controller	GND		VINT	

Table 7: Recommended Operation Conditions

6. Functional Block Diagram

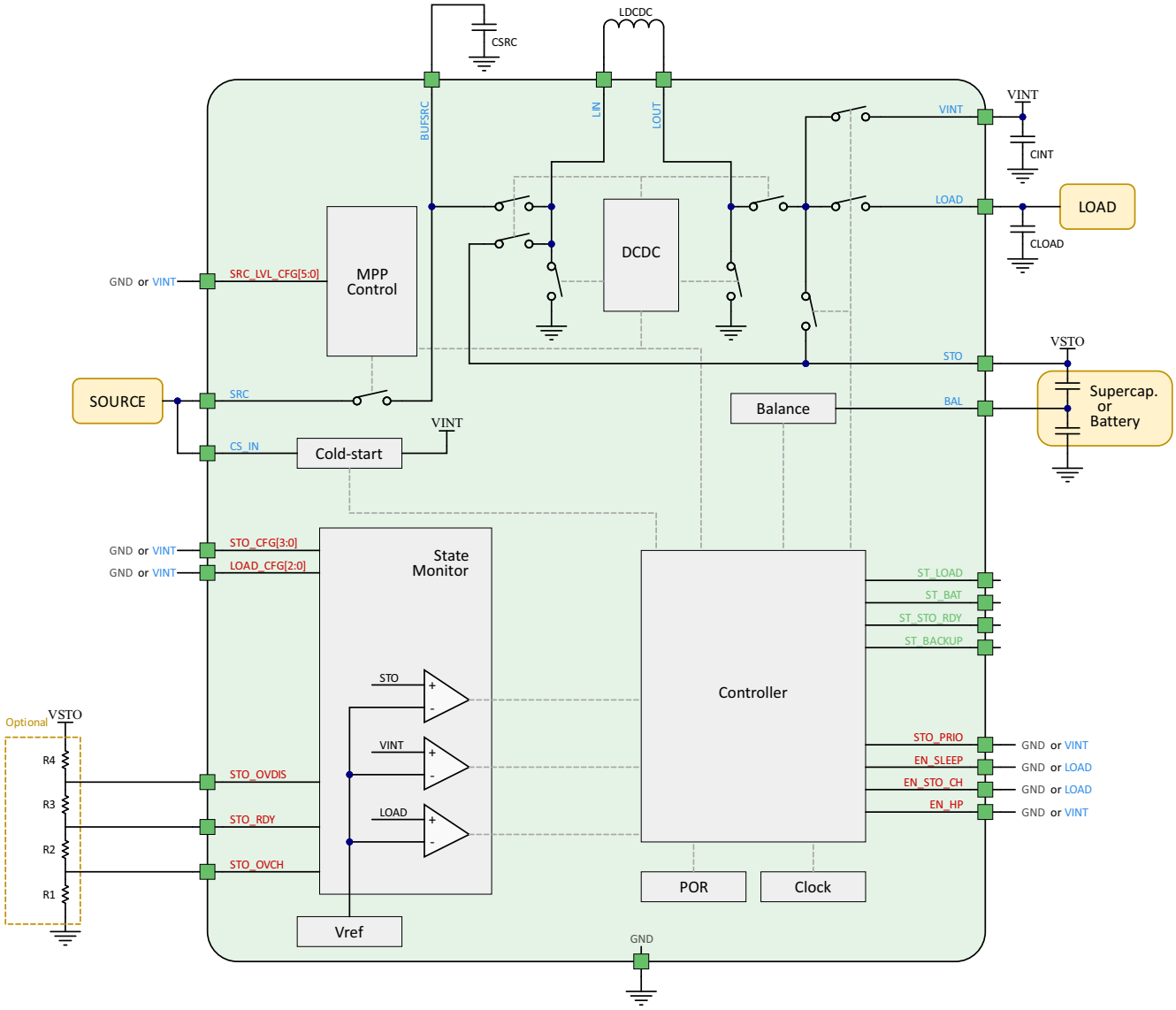

Figure 3: Functional Block Diagram

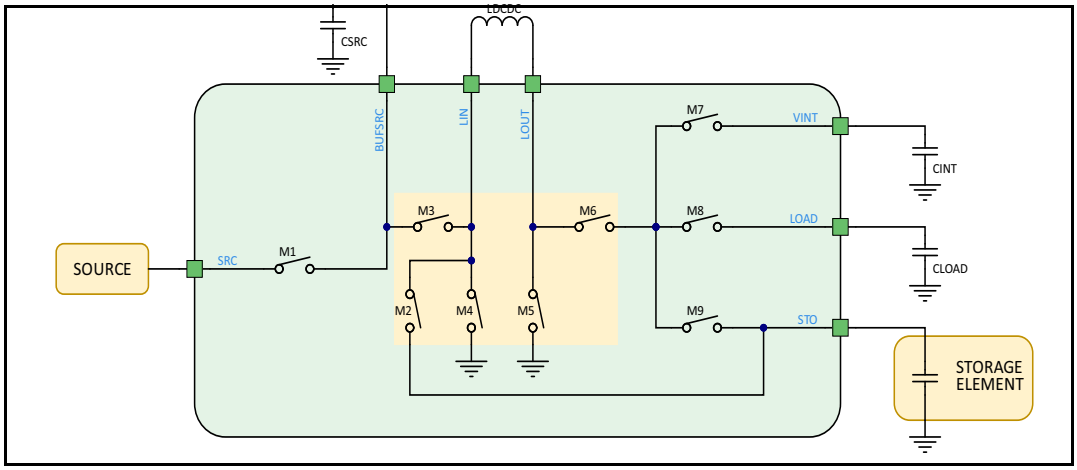

Figure 4: Simplified Schematic View of the AEM00330

7. Theory of Operation

7.1. DCDC Converter

The DCDC converter converts the voltage available at BUFSRC or at STO to a level suitable for charging the storage element STO or to regulate the LOAD and the internal supply VINT. The switching transistors of the DCDC converter are M2 or M3, M4, M5 and M6. Thanks to M7, M8 and M9, the controller selects between LOAD, STO and VINT respectively as the converter output. M1 selects the source as main input of energy. The internal supply VINT is regulated with priority over LOAD. STO is selected as an output only when neither VINT nor LOAD needs to be supplied. The converter has two possible inputs: BUFSRC or STO. BUFSRC is used by default as an input via M3. If the energy available on SRC is not sufficient to maintain the LOAD or VINT voltage, for instance because of a sudden current peak on LOAD, the converter uses STO instead as an input via M2 to keep LOAD and VINT regulated.

The reactive power component of this converter is the external inductor LDCDC. V_{SRC} is regulated to $V_{SRC,REG}$ configured by SRC_LVL_CFG[5:0]. BUFSRC is decoupled by the capacitor CSRC, which smooths the voltage against the current pulses pulled by the DCDC converter. The storage element is connected to the STO pin.

Depending on its input voltage and its output voltage, the DCDC converter will work as a boost converter, a buck converter or a buck-boost converter. The maximum power that can be harvested and supplied to the output LOAD depends on the power mode (HIGH POWER MODE or LOW POWER MODE), which is configured through the EN_HP pin (see Section 8.1).

DCDC converter mode	Input Voltage / Output Voltage
Boost	$V_{IN} < V_{OUT}$ - 250mV
Buck	$V_{IN} > V_{OUT}$ + 250 mV
Buck - Boost	V_{OUT} - 250mV < V_{IN} < V_{OUT} + 250mV

Table 8: DCDC Converter Modes

7.2. Reset, Wake Up and Start States

The RESET STATE is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold start voltage of 275 mV and a sparse amount of power of just 3 µW become available on CS_IN (usually connected to SRC), the AEM00330 switches to WAKE-UP STATE, and energy is extracted from SRC to make V_{VINT} rise to 2.2 V. When V_{VINT} reaches those 2.2 V, the AEM00330 switches to START STATE. In START STATE, two scenarios are possible: in the first scenario, STO_PRIO is asserted, the storage element connected to STO has the priority on the one connected to LOAD. In the second scenario, STO_PRIO is reset and the LOAD has the priority.

When the AEM00330 is in RESET STATE, WAKE-UP STATE or START STATE, the DCDC converter's input is always BUFSRC: STO is never used as input. This guarantees that the storage element is not used until a minimum amount of energy has been stored in it.

7.2.1. Storage Element Priority

This paragraph covers the AEM00330 behaviour when STO_PRIO is pulled up to VINT, so that the storage element connected on STO has priority over LOAD.

Supercapacitor as a Storage Element

If the storage element is a supercapacitor, it may be fully discharged at first and thus need to be charged from 0 V. The DCDC converter charges STO from the input source (SRC). When V_{STO} reaches V_{CHRDY}, the circuit enters SUPPLY STATE.

Battery as a Storage Element

If the storage element is a battery, but its voltage is lower than V_{CHRDY}, then the storage element needs to be charged first until it reaches V_{CHRDY}. Once V_{STO} reaches V_{CHRDY}, or if the battery was initially charged above V_{CHRDY}, the circuit enters SUPPLY STATE.

7.2.2. Load Priority

If STO_PRIO is connected to GND, the AEM charges first the LOAD to $V_{LOAD,MAX}$ (see Table 10) using energy from the source (SRC). This allows to first supply the application circuit connected to LOAD. If the storage element was initially charged above V_{CHRDY}, the circuit enters SUPPLY STATE as soon as LOAD reaches $V_{LOAD,TYP}$. If the storage element is a supercapacitor or a battery which voltage is lower than V_{CHRDY}, the AEM keeps regulating LOAD between $V_{LOAD,MAX}$ and $V_{LOAD,TYP}$. Meanwhile, any excess charges on the source is used to charge the storage element until it reaches V_{CHRDY}. Once V_{STO} exceeds V_{CHRDY}, the circuit enters into SUPPLY STATE.

This configuration is useful when a large storage element is connected to STO and a smaller one is connected to LOAD: the application starts as soon as CLOAD is charged and does not have to wait for the large storage element on STO to be charged.

7.3. Supply State

In SUPPLY STATE, four scenarios are possible:

- There is enough power provided by the source (SRC) to keep V_{LOAD} near $V_{LOAD,TYP}$ with a small hysteresis and V_{VINT} at 2.2 V. The excessive power is used to charge the storage element on STO. In that case, the circuit remains in SUPPLY STATE. If STO is fully charged, LOAD will be maintained at $V_{LOAD,MAX}$ instead of $V_{LOAD,TYP}$.
- If the circuit connected to LOAD consumes more energy than the energy that the AEM00330 is able to extract from the source, the LOAD circuit will be supplied by the storage element connected to the STO terminal. In this case, the circuit stays in SUPPLY STATE.
- Due to a lack of power from the source, V_{STO} falls below V_{OVDIS}. In this case, the circuit enters SHUTDOWN STATE as explained in Section 7.4.
- If EN_SLEEP is asserted and conditions (shown on Figure 5) on V_{LOAD} and V_{VINT} are satisfied, the AEM enters SLEEP STATE (see section 7.5).

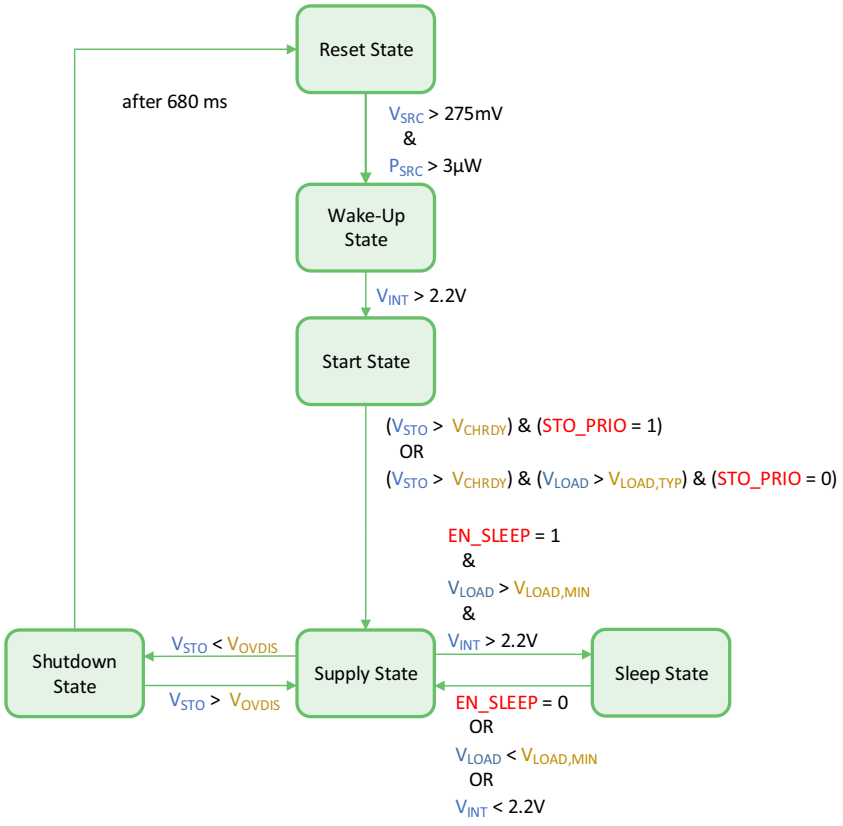

Figure 5: Diagram of the AEM00330 States

7.4. Shutdown State

If the storage element gets depleted (V_{STO} < V_{OVDIS}), the AEM00330 goes to SHUTDOWN STATE. As long as the AEM00330 is in this state, the ST_STO_OVDIS is asserted. In SHUTDOWN STATE, if V_{STO} recovers within 680 ms, the AEM00330 goes back to SUPPLY STATE. This prevents false detection of the storage element being empty because of a LOAD current peak.

7.5. Sleep State

SLEEP STATE reduces the AEM00330 quiescent current by disabling the DCDC converter and by reducing the controller clock frequency. If VINT voltage or V_{LOAD} fall below their regulation value, the AEM00330 temporarily exits SLEEP STATE to wake up the DCDC converter and supply VINT or LOAD. Exiting SLEEP STATE and waking up the DCDC converter takes up to 1 ms. Depending on the expected LOAD current, CLOAD value must be adapted to act as an energy buffer during the 1 ms required to wake up the DCDC converter. Therefore, this mode should be used when LOAD current is small. As the DCDC is enabled, no energy is harvested from SRC while in SLEEP STATE.

The AEM00330 enters SLEEP STATE if **all** the following conditions are satisfied:

- EN_SLEEP pin pulled up to LOAD
- V_{VINT} > 2.2 V
- V_{LOAD} > $V_{LOAD,TYP}$

The AEM00330 leaves SLEEP STATE and switches back to SUPPLY STATE if **one** of the following conditions is satisfied:

- EN_SLEEP pin pulled down to GND
- V_{VINT} < 2.2 V
- V_{LOAD} < $V_{LOAD,TYP}$

The AEM00330 will then stay in SUPPLY STATE until the SLEEP STATE conditions are all satisfied again.

7.6. Source Voltage Regulation

During SUPPLY STATE, the voltage on SRC is regulated to a voltage configured by the user. The AEM00330 offers a choice of fifty-nine values for the source voltage. If the open-circuit voltage of the harvester is lower than $V_{SRC,REG}$, the AEM00330 does not extract the power from the source. If the SRC voltage is higher, the AEM00330 regulates V_{SRC} to $V_{SRC,REG}$ and extracts power.

7.7. Balancing for Dual-Cell Supercapacitor

The balancing circuit allows the user to balance the internal voltage of the dual-cell supercapacitor connected to STO in order to avoid damaging the supercapacitor because of excessive voltage on one cell.

If BAL is connected to GND, the balancing circuit is disabled. This configuration must be used if a battery, a capacitor or a single-cell supercapacitor is connected on STO.

If BAL is connected to the node between both cells of a supercapacitor, the balancing circuit compensates for any mismatch of the two cells that could lead to the over-charge of one of two cells. The balancing circuit ensures that BAL remains close to V_{STO} / 2. This configuration must be used if a dual-cell supercapacitor is connected to STO, and that this supercapacitor requires cells balancing.

8. System Configuration

8.1. High Power / Low Power Mode

When EN_HP is pulled to VINT, the DCDC converter is configured to HIGH POWER MODE. This allows higher currents to be extracted from the DCDC converter input (SRC or STO) to the DCDC converter output (LOAD or STO). Figure 6 shows the maximum current that the DCDC converter can supply to LOAD, depending on the storage voltage V_{STO}, for every available load voltage V_{LOAD}, for both HIGH POWER MODE and LOW POWER MODE.

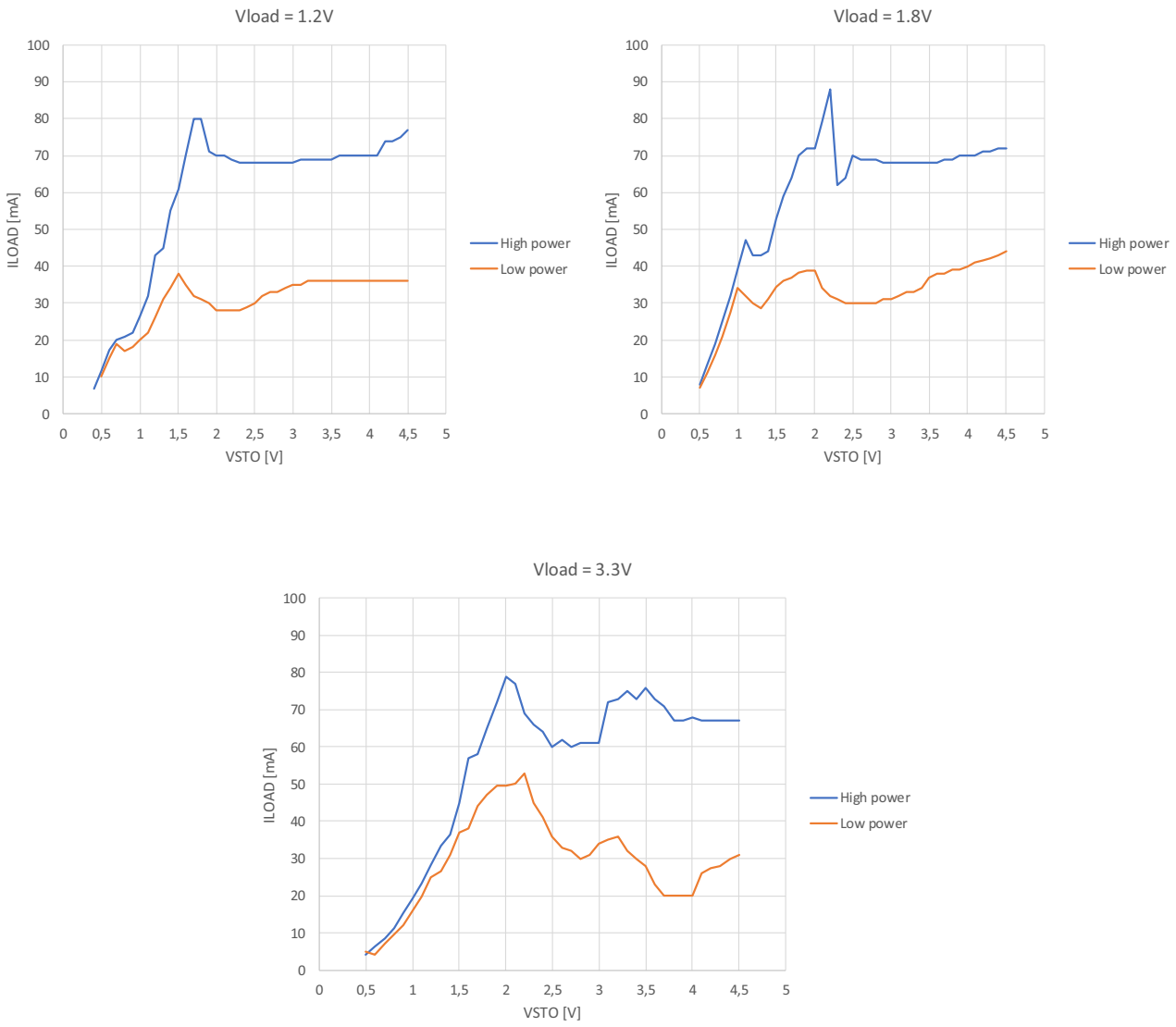

Figure 6: Maximum LOAD Current Depending on V_{STO} and on V_{LOAD}

8.2. Storage Element Configuration

Through four configuration pins (STO_CFG[3:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 9. The three threshold levels are defined as:

- V_{OVCH}: maximum voltage accepted on the storage element before disabling its charging.
- V_{CHRDY}: minimum voltage required on the storage element before starting to supply the LOAD (if STO_PRIO is asserted) and entering supply state after start-up.
- V_{OVDIS}: minimum voltage accepted on the storage element before considering the storage element as depleted resetting ST_STO.

A large-size storage element is not mandatory on STO:

- If the harvested energy source is permanently available and covers the application needs or
- If the application does not need to store energy when the harvested energy source is not available

The storage element may then be replaced by an external capacitor CSTO with a minimum value of 100 µF.

CAUTION: running the AEM00330 without this 100 µF minimum capacitance on STO will permanently damage the circuit.

Configuration pins				Storage element threshold voltages			Typical use
STO_CFG[3]	STO_CFG[2]	STO_CFG[1]	STO_CFG[0]	V_{OVDIS}	V_{CHRDY}	V_{OVCH}	
0	0	0	0	3.00 V	3.50 V	4.05 V	Li-ion battery
0	0	0	1	2.80 V	3.10 V	3.60 V	LiFePO4 battery
0	0	1	0	1.85 V	2.40 V	2.70 V	NiMH battery
0	0	1	1	0.20 V	1.00 V	4.65 V	Dual-cell supercapacitor
0	1	0	0	0.20 V	1.00 V	2.60 V	Single-cell supercapacitor
0	1	0	1	1.00 V	1.20 V	2.95 V	Single-cell supercapacitor
0	1	1	0	1.85 V	2.30 V	2.60 V	NGK
0	1	1	1	Custom Mode			
1	0	0	0	1.10 V	1.25 V	1.50 V	Ni-Cd 1 cells
1	0	0	1	2.20 V	2.50 V	3.00 V	Ni-Cd 2 cells
1	0	1	0	1.45 V	2.00 V	4.65 V	Dual-cell supercapacitor
1	0	1	1	1.00 V	1.20 V	2.60 V	Single-cell supercapacitor
1	1	0	0	2.00 V	2.30 V	2.60 V	ITEN / Umal Murata
1	1	0	1	3.00 V	3.50 V	4.35 V	Li-Po battery
1	1	1	0	2.60 V	2.70 V	4.00 V	Tadiran TLI1020A
1	1	1	1	2.60 V	3.50 V	3.90 V	Tadiran HLC1020

Table 9: Storage Element Configuration Pins

8.3. Load Configuration

The LOAD output voltage V_{LOAD} can be configured thanks to the LOAD_CFG[2:0] configuration pins covering most application cases (see Table 10). V_{LOAD} is regulated to $V_{LOAD,TYP}$. However, if V_{LOAD} falls below $V_{LOAD,MID}$, the controller forces STO as an input of the DCDC converter to supply LOAD.

Configuration pins			LOAD output voltage			
LOAD_CFG[2]	LOAD_CFG[1]	LOAD_CFG[0]	$V_{LOAD,MIN}$	$V_{LOAD,MID}$	$V_{LOAD,TYP}$	$V_{LOAD,MAX}$
0	0	0	3.15 V	3.23 V	3.28 V	3.34 V
0	0	1	2.35 V	2.47 V	2.50 V	2.53 V
0	1	0	1.64 V	1.75 V	1.79 V	1.82 V
0	1	1	1.14 V	1.16 V	1.20 V	1.23 V
1	0	0	1.39 V	1.56 V	1.61 V	2.63 V
1	0	1	1.39 V	1.56 V	1.61 V	4.65 V
1	1	0	Reserved, do not use			
1	1	1				

Table 10: Load Configuration Pins

8.4. Custom Mode Configuration

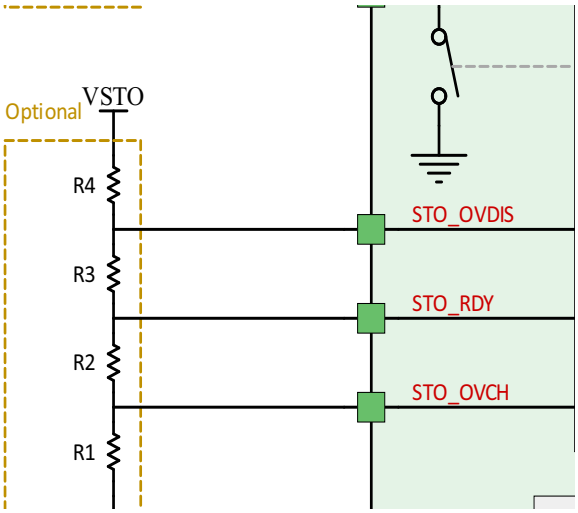

Figure 7: Custom Mode Settings

When STO_CFG[3:0] = 0111, the custom mode is selected and all four configuration resistors must be wired as shown in Figure 25.

V_{OVCH}, V_{CHRDY} and, V_{OVDIS} are defined thanks to R1, R2, R3 and R4, which can be determined within the following constraints:

- RT = R1 + R2 + R3 + R4
- 1 MΩ ≤ RT ≤ 100 MΩ
- R1 = RT (1 V / V_{OVCH})
- R2 = RT (1 V / V_{CHRDY} - 1 V / V_{OVCH})
- R3 = RT (1 V / V_{OVDIS} - 1 V / V_{CHRDY})
- R4 = RT (1 - 1 V / V_{OVDIS})

The resistors should have high values to make the additional power consumption negligible. Moreover, the following constraints must be respected to ensure the functionality of the chip:

- V_{CHRDY} + 0.05 V ≤ V_{OVCH} ≤ 4.5 V
- V_{OVDIS} + 0.05 V ≤ V_{CHRDY} ≤ V_{OVCH} - 0.05 V
- 1V ≤ V_{OVDIS}

8.5. Disable Storage Element Charging

Pulling down EN_STO_CH pin to GND disables the charging of the storage element connected to STO from SRC. This can be done for example to protect the storage element when the system detects that the environment temperature is too low or too high to safely charge the storage element.

While EN_STO_CH is pulled down, VINT and LOAD can still be supplied either from SRC or from STO.

To enable charging the storage element on STO, EN_STO_CH must be pulled up to LOAD or left floating (pin is pulled up internally).

NOTE: STO will still be charged to V_{CHRDY} during the START STATE

8.6. Source Level Configuration

Six dedicated configuration pins, SRC_LVL_CFG[5:0], allow selecting the $V_{SRC,REG}$ at which the source regulates its voltage.

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
0	0	0	0	0	0	0.14 V
0	0	0	0	0	1	0.17 V
0	0	0	0	1	0	0.20 V
0	0	0	0	1	1	0.23 V
0	0	0	1	0	0	0.26 V
0	0	0	1	0	1	0.30 V
0	0	0	1	1	0	0.34 V
0	0	0	1	1	1	0.39 V
0	0	1	0	0	0	0.43 V
0	0	1	0	0	1	0.48 V
0	0	1	0	1	0	0.52 V
0	0	1	0	1	1	0.57 V
0	0	1	1	0	0	0.61 V
0	0	1	1	0	1	0.66 V
0	0	1	1	1	0	0.70 V
0	0	1	1	1	1	0.75 V
0	1	0	0	0	0	0.80 V
0	1	0	0	0	1	0.84 V
0	1	0	0	1	0	0.89 V
0	1	0	0	1	1	0.95 V
0	1	0	1	0	0	1.05 V
0	1	0	1	0	1	1.14 V
0	1	0	1	1	0	1.23 V
0	1	0	1	1	1	1.32 V
0	1	1	0	0	0	1.41 V
0	1	1	0	0	1	1.50 V
0	1	1	0	1	0	1.59 V

Table 11: Source regulation Configuration Pins

Configuration pins						Voltage Level
SRC_LVL_CFG[5:0]						$V_{SRC,REG}$
0	1	1	0	1	1	1.68 V
0	1	1	1	0	0	1.77 V
0	1	1	1	0	1	1.86 V
0	1	1	1	1	0	1.95 V
0	1	1	1	1	1	2.05 V
1	0	0	0	0	0	2.14 V
1	0	0	0	0	1	2.23 V
1	0	0	0	1	0	2.32 V
1	0	0	0	1	1	2.41 V
1	0	0	1	0	0	2.50 V
1	0	0	1	0	1	2.59 V
1	0	0	1	1	0	2.68 V
1	0	0	1	1	1	2.77 V
1	0	1	0	0	0	2.86 V
1	0	1	0	0	1	2.95 V
1	0	1	0	1	0	3.05 V
1	0	1	0	1	1	3.14 V
1	0	1	1	0	0	3.23 V
1	0	1	1	0	1	3.32 V
1	0	1	1	1	0	3.41 V
1	0	1	1	1	1	3.50 V
1	1	0	0	0	0	3.59 V
1	1	0	0	0	1	3.68 V
1	1	0	0	1	0	3.77 V
1	1	0	0	1	1	3.86 V
1	1	0	1	0	0	3.95 V
1	1	0	1	0	1	4.05 V
1	1	0	1	1	0	4.14 V
1	1	0	1	1	1	4.23 V
1	1	1	0	0	0	4.32 V
1	1	1	0	0	1	4.41 V
1	1	1	0	1	0	4.50 V

Table 11: Source regulation Configuration Pins

8.7. External Components

Refer to Figure 44 to have an illustration of the external components wiring.

8.7.1. Storage element information

The energy storage element of the AEM00330 can be a rechargeable battery, a supercapacitor or a capacitor. The size of the storage element must be determined so that its voltage does not fall below V_{OVDIS} even during current peaks pulled by the application circuit connected to LOAD. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to decouple the battery with a capacitor.

If the application expects a disconnection of the battery (e.g. because of a user removable connector), the PCB should include a capacitor CSTO of at least 100 µF connected between STO and GND. The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the whole subsystem.

8.7.2. External inductor information

The AEM00330 operates with one standard miniature inductor. LDCDC must sustain a peak current of at least 1 A and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) favours the power conversion efficiency of the DCDC converter. The recommended value is 10 µH.

8.7.3. External capacitors information

CSRC

This capacitor acts as an energy buffer at the input of the DCDC converter. It prevents large voltage fluctuations when the DCDC converter is switching. The recommended value is 15 µF.

CINT

This capacitor acts as an energy buffer for the internal voltage supply. The recommended value is 10 µF.

CLOAD

This capacitor acts as an energy buffer for LOAD. It also reduces the voltage ripple induced by the current pulses inherent to the switched behaviour of the converter. The recommended value is at least 40 µF.

9. Typical Application Circuits

9.1. Example Circuit 1

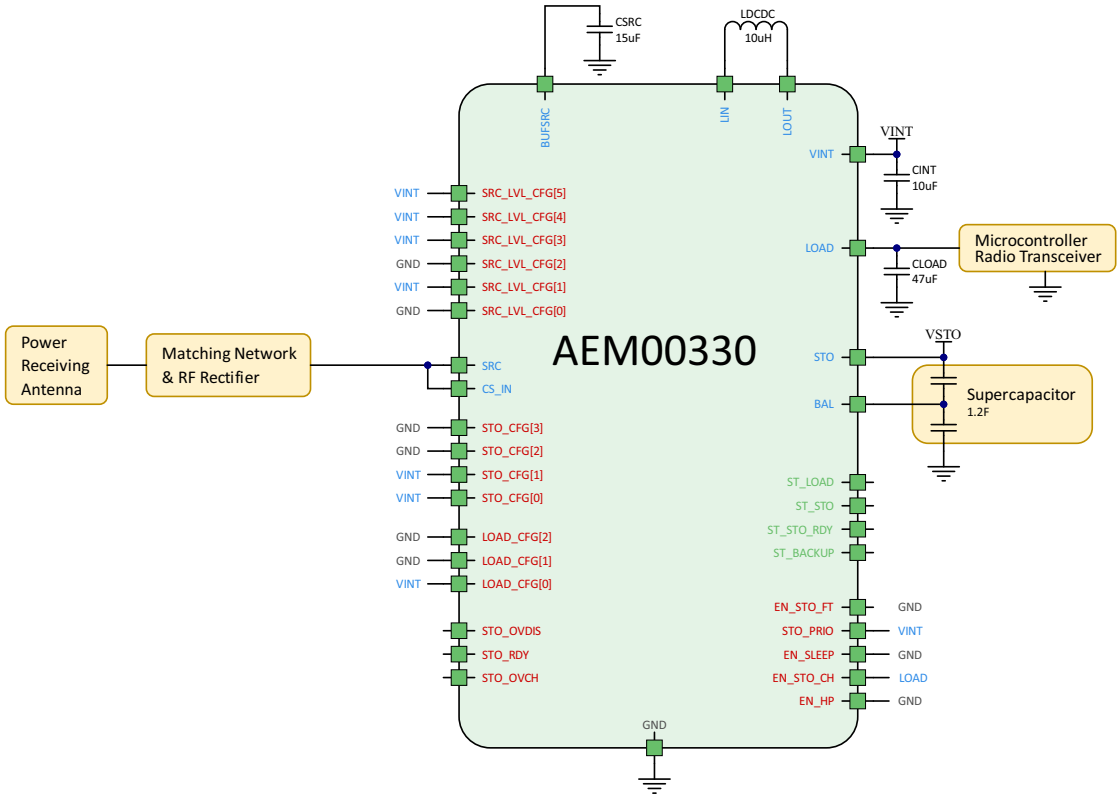

Figure 8: Typical Application Circuit 1

The circuit is an example of a system with Radio Frequency (RF) energy harvesting. It uses a pre-defined operating mode that uses standard components, and a supercapacitor as energy storage.

- Energy source: RF source
- SRC_LVL_CFG[5:0] = 111010: the AEM00330 starts to extract power from 4.5V and regulates V_{SRC} to 4.5V.
- STO_CFG[3:0] = 0011: the storage element is a dual-cell supercapacitor, with:
  - V_{OVCH} = 4.65 V
  - V_{CHRDY} = 1.00 V
  - V_{OVDIS} = 0.20 V
- The balancing pin of the dual-cell supercapacitor is connected to BAL
- LOAD_CFG[2:0] = 001: the microcontroller and the radio transceiver are supplied by the LOAD terminal, which is regulated at V_{LOAD} = 2.5 V
- STO_PRIO is connected to VINT: at start-up STO will be charged and before LOAD
- EN_SLEEP is connected to GND: the AEM00330 will never switch to SLEEP STATE
- EN_STO_CH is connected to GND : the charging of the storage element on STO is disabled
- EN_HP is connected to GND: the DCDC converter is in LOW POWER MODE

9.2. Example Circuit 2

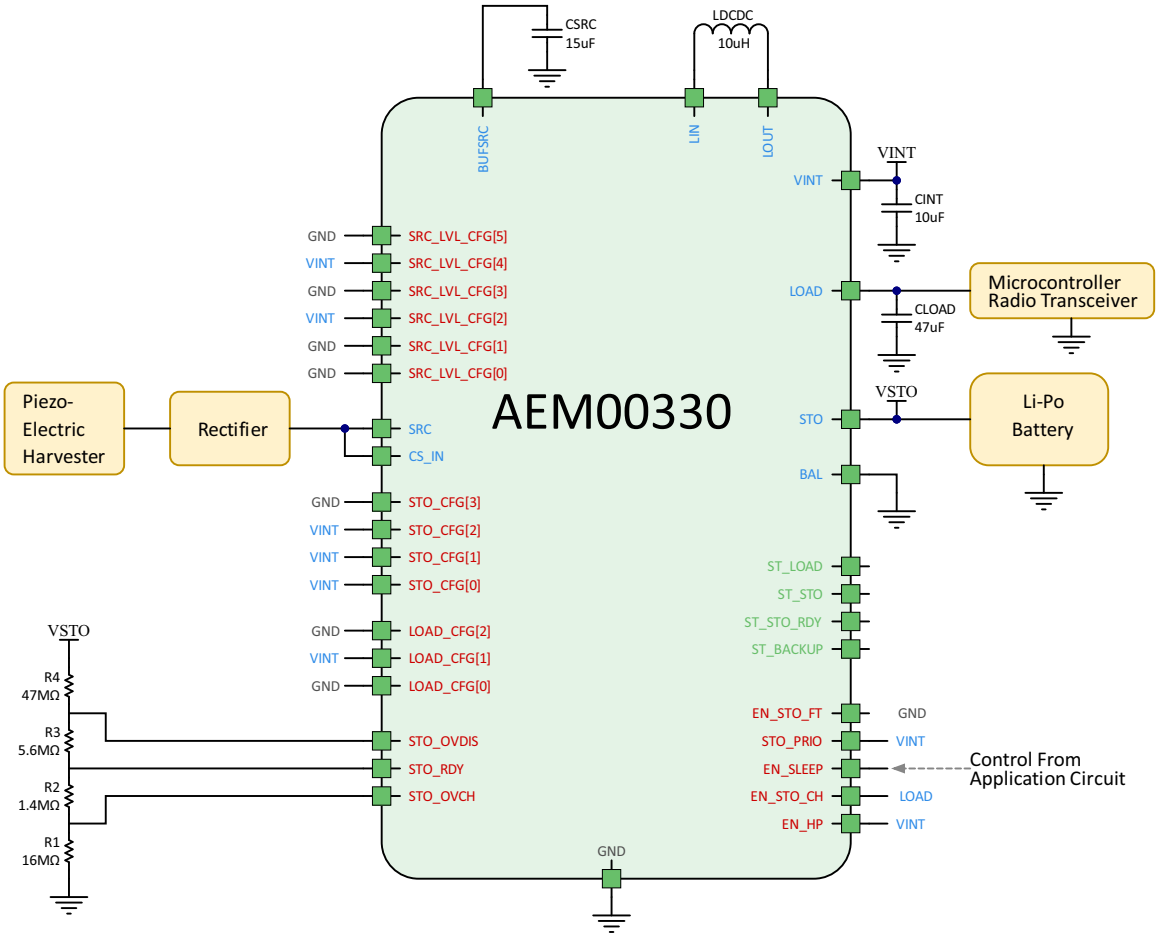

Figure 9: Typical Application Circuit 2

The circuit is an example of a system with vibration energy harvesting. It uses a Li-Po rechargeable battery as energy storage, which voltages thresholds are set by the custom mode.

Please note that the custom mode is used for the sake of the example, but most applications that use a Li-Po battery as storage element could use a pre-defined mode that does not require to implement the resistive divider (R1-R2-R3-R4), and thus have a reduced bill of materials compared to the circuit shown on Figure 20.

- Energy source: piezoelectric vibration harvester
- SRC_LVL_CFG[5:0] = 010100: the AEM00330 starts to extract power from 1.05V and regulates V_{SRC} to 1.05V.
- STO_CFG[3:0] = 0111: the storage element is a Li-Po rechargeable battery, used with custom mode (in this example we set V_{CHRDY} to 4.0V instead of the 3.51V on STO_CFG[3:0] = 1101 preset):
  - V_{OVCH} = 4.35V
  - V_{CHRDY} = 4.00V
  - V_{OVDIS} = 3.03V
- Custom mode resistor divider calculations (values have been rounded to the closest available value):
  - RT = 70MΩ
  - R1 = 70MΩ * (1V / 4.35V) ≈ 16MΩ
  - R2 = 70MΩ * (1V / 4.00V - 1V / 4.35V) ≈ 1.4MΩ
  - R3 = 70MΩ * (1V / 3.03V - 1V / 4.00V) ≈ 5.6MΩ
  - R4 = 70MΩ * (1 - 1V / 3.03V) ≈ 47MΩ
- BAL is not used (not a dual-cell storage element) so it is connected to GND.
- LOAD_CFG[2:0] = 010: the micro-controller and the radio transceiver are supplied by the LOAD terminal, which is regulated at V_{LOAD} = 1.8V

- STO_PRIO is connected to VINT: at start-up STO will be charged and before LOAD
- EN_SLEEP is controlled by the application circuit, typically by a microcontroller GPIO output
- connected to LOAD: the charging of the storage element present on STO is enabledEN_HP is connected to VINT: the DCDC converter is in HIGH POWER MODE

9.3. Circuit Behaviour

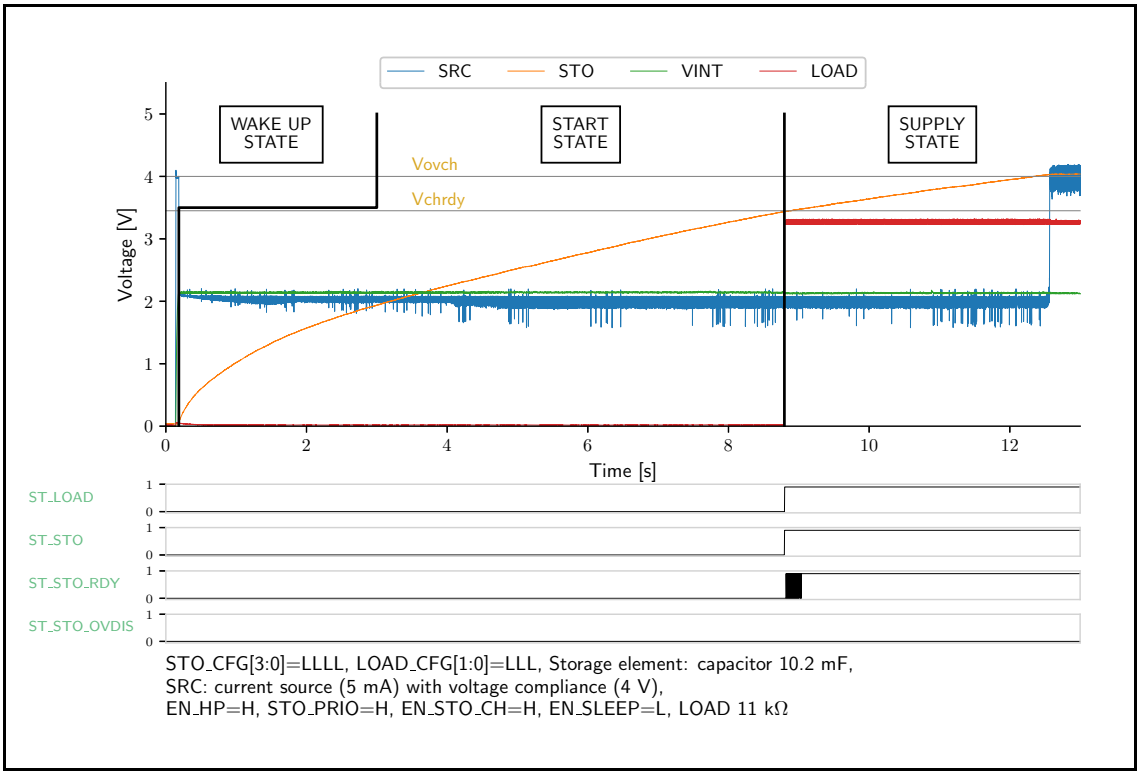

Figure 10: Wake-up state, Start state and Supply state

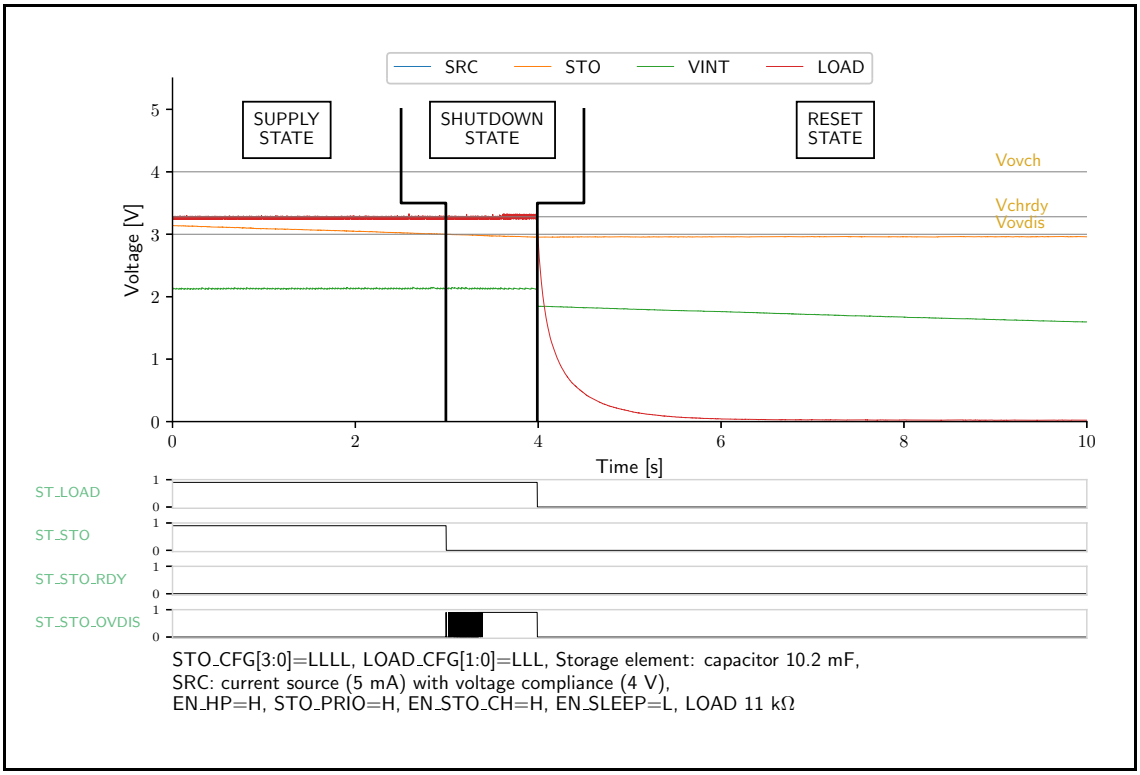

Figure 11: Wake-up state, Start state and Supply state

9.4. DCDC Conversion Efficiency From SRC to STO in Low Power Mode

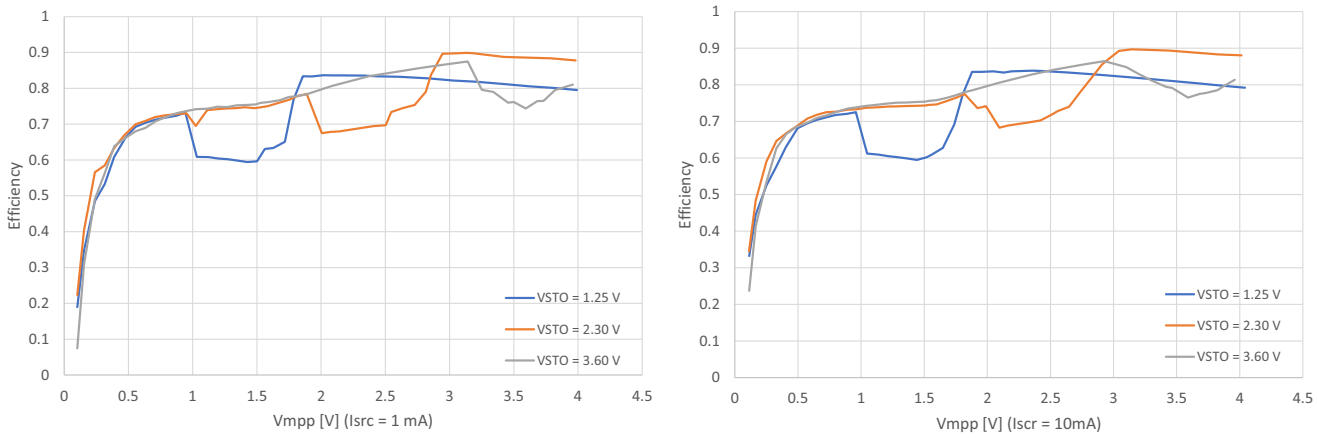

Figure 12: DCDC Efficiency from SRC to STO for 1 mA and 10 mA in Low Power Mode

9.5. DCDC Conversion Efficiency From SRC to STO in High Power Mode

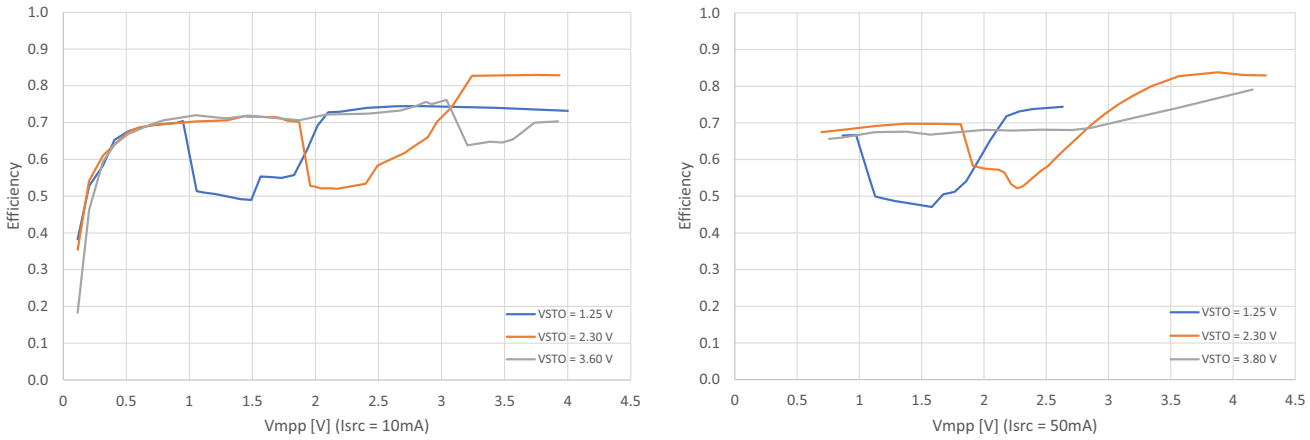

Figure 13: DCDC Efficiency from SRC to STO for 10 mA and 50 mA in High Power Mode

9.6. DCDC Conversion Efficiency From STO to LOAD in Low Power Mode

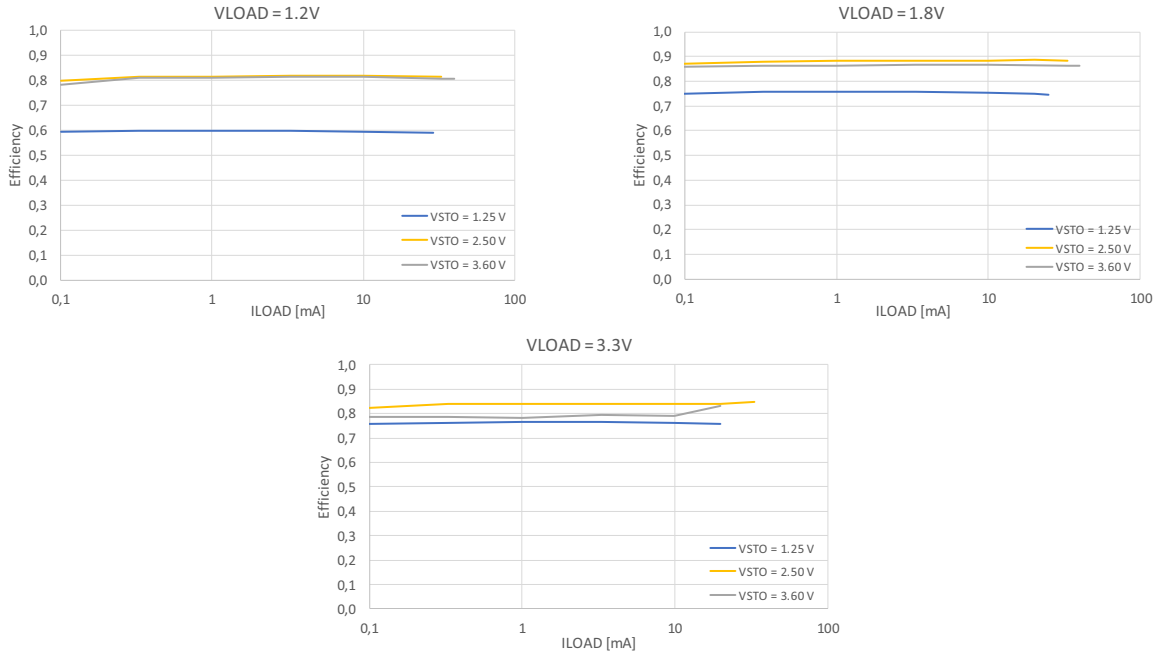

Figure 14: DCDC Efficiency from STO to LOAD in Low Power Mode

9.7. DCDC Conversion Efficiency From STO to LOAD in High Power Mode

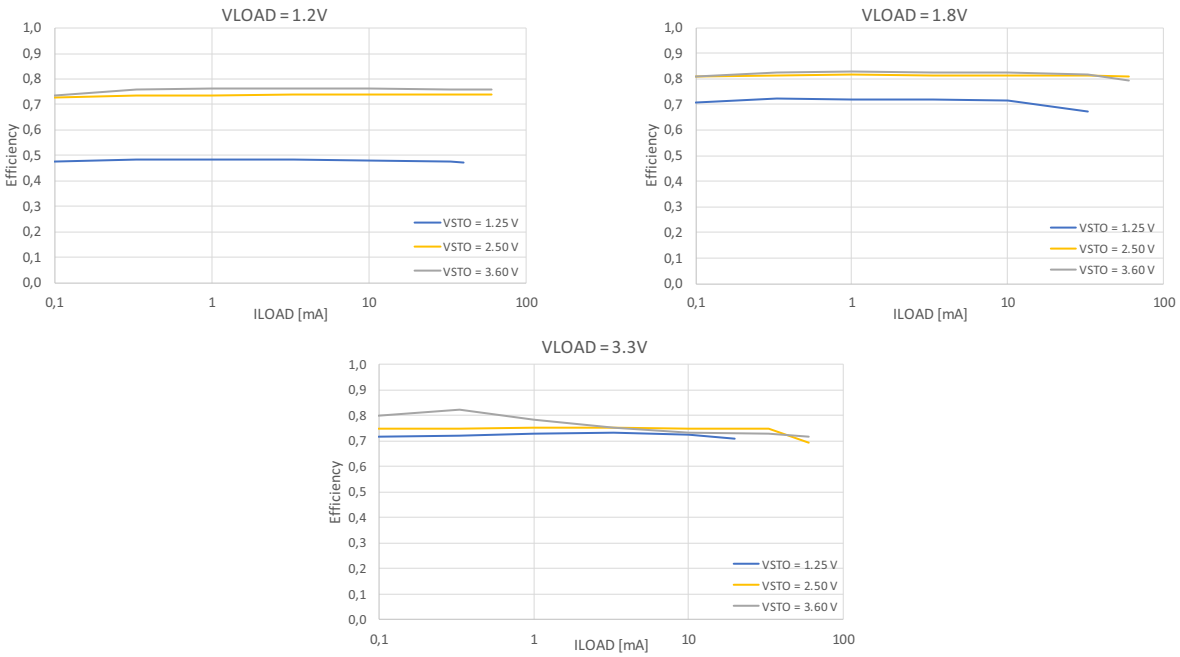

Figure 15: DCDC Efficiency from STO to LOAD in High Power Mode

10. Schematic

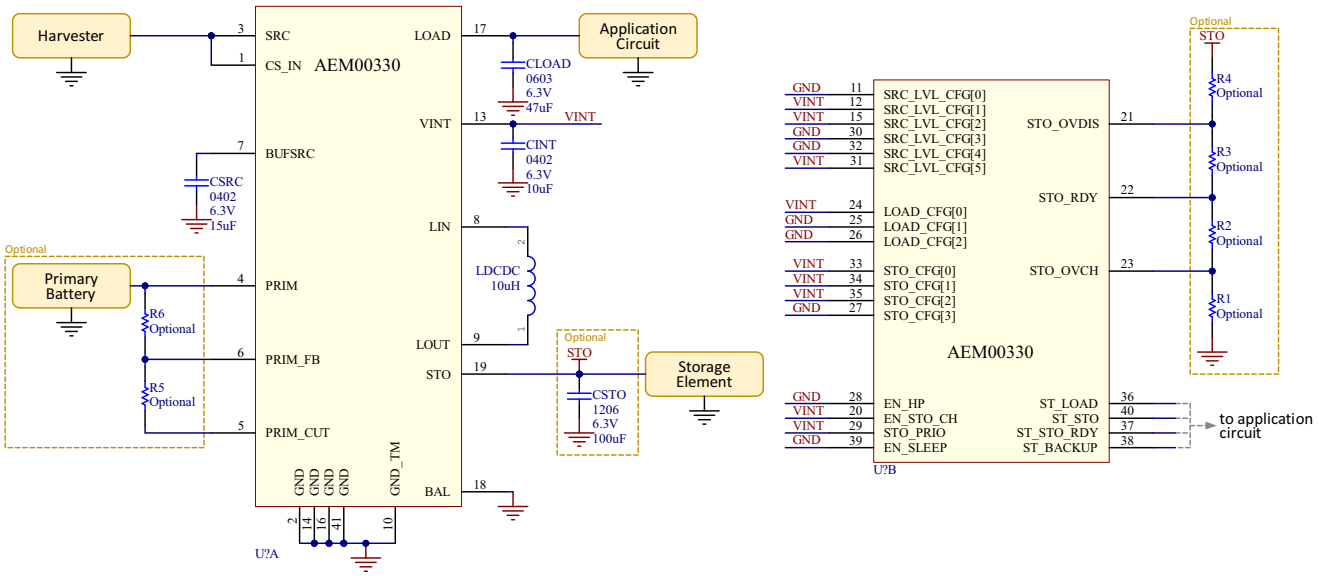

Figure 16: Schematic Example

Designator	Description	Quantity	Manufacturer	Link
U1	AEM00330 - Symbol QFN 40-pin	1	e-peas	order at sales@e-peas.com
LDCDC	Power inductor 10 µH - 1.76A	1	Murata	DFE252010F-100M
CLOAD	Ceramic Cap 47 µF, 6.3V, 20%, X5R 0603	1	Murata	GRM188R60J476ME15
CINT	Ceramic Cap 10 µF, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J106ME15
CSRC	Ceramic Cap 15 µF, 6.3V, 20%, X5R 0402	1	Murata	GRM155R60J156ME05
CSTO (optional)	Ceramic Cap 100 µF, 6.3V, 20%, X5R 1206	1	TDK	C3216X5R1A107M160AC

Table 12: Minimal Bill of Materials

11. Layout

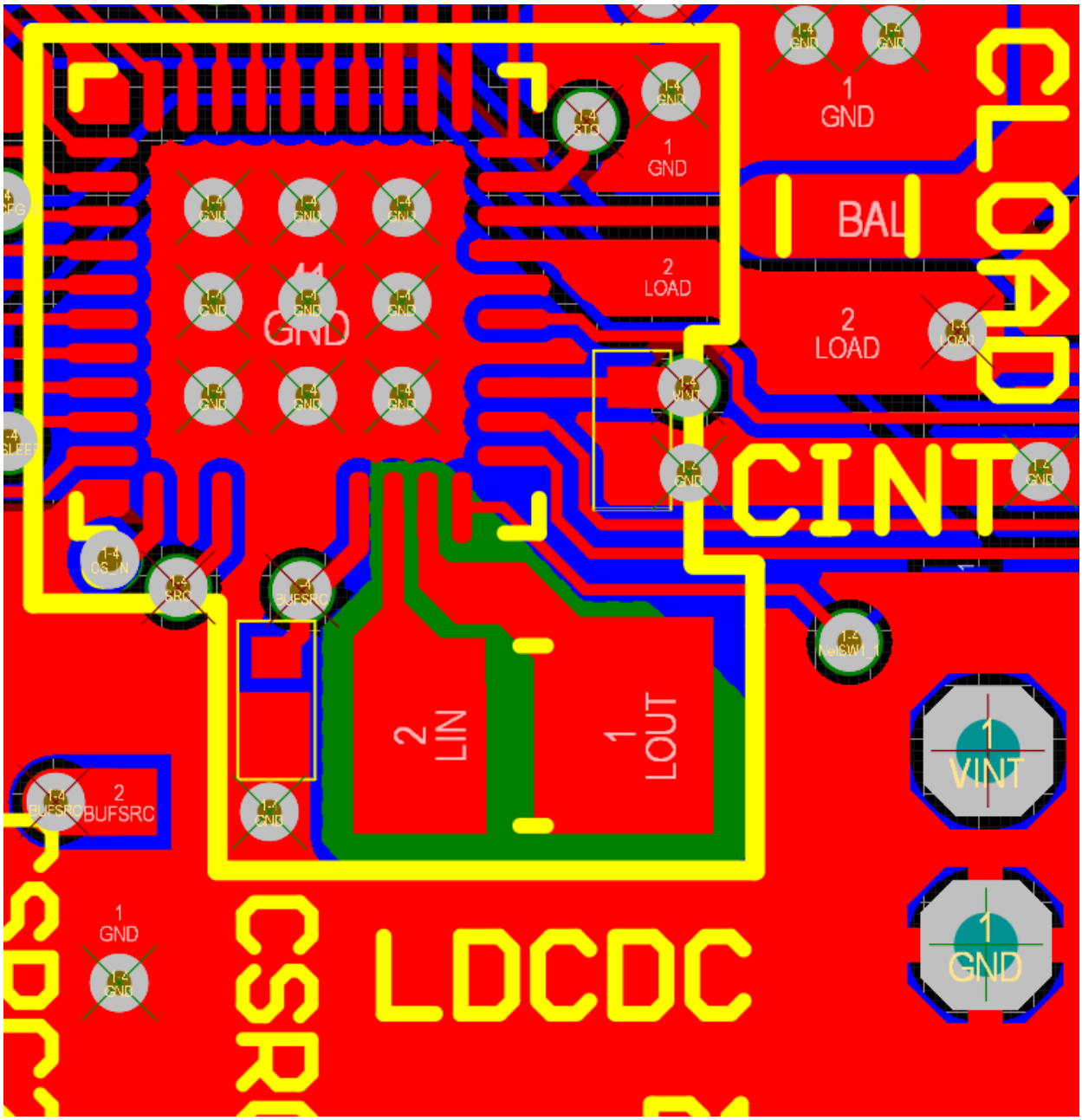

Figure 17: Layout Example for the AEM00330 and its Passive Components

NOTE: schematic, symbol and footprint for the e-peas component can be ordered by contacting e-peas support team at support@e-peas.com

12. Package Information

12.1. Plastic Quad Flatpack No-Lead (QFN 40-pin 5x5mm)

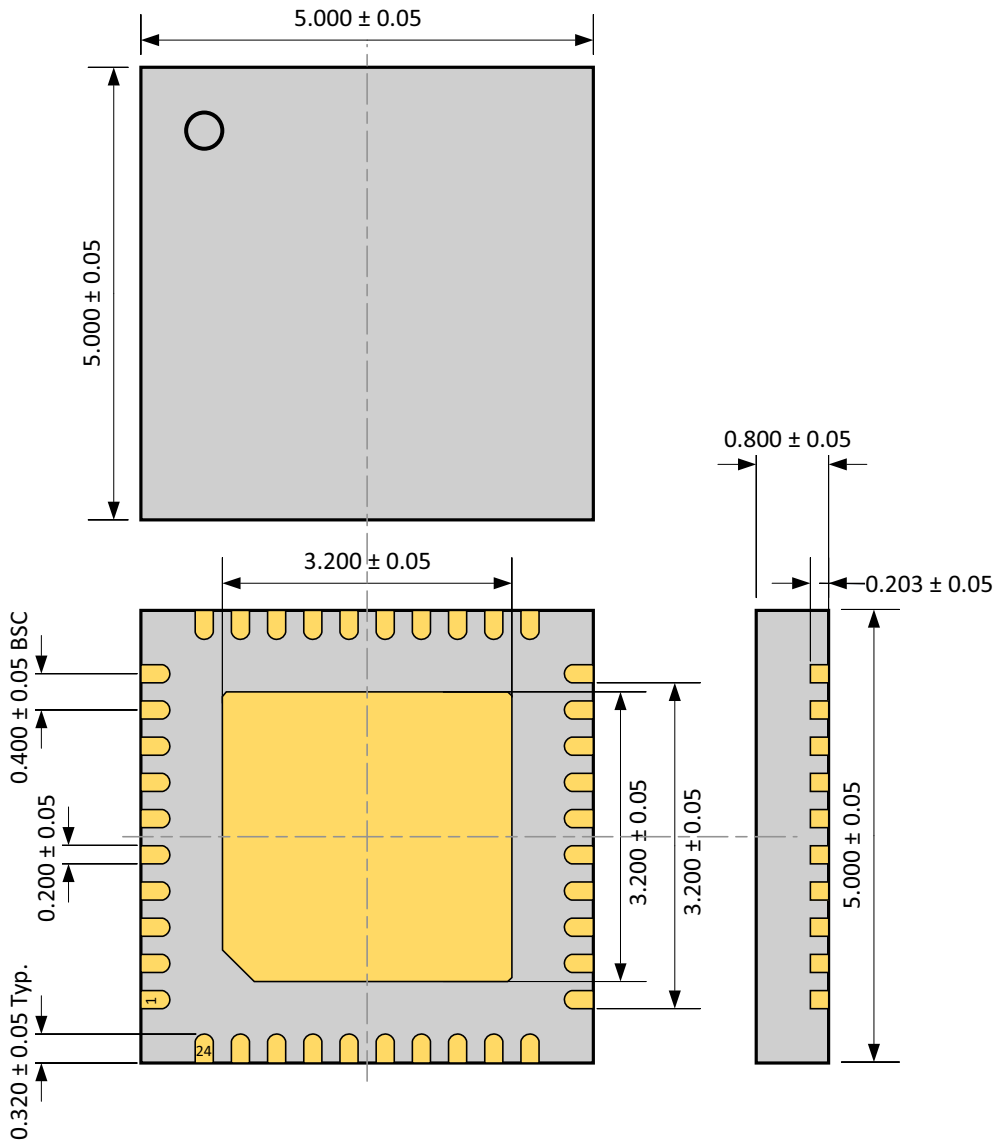

Figure 18: QFN 40-pin 5x5mm Drawing (All Dimensions in mm)

12.2. Board Layout

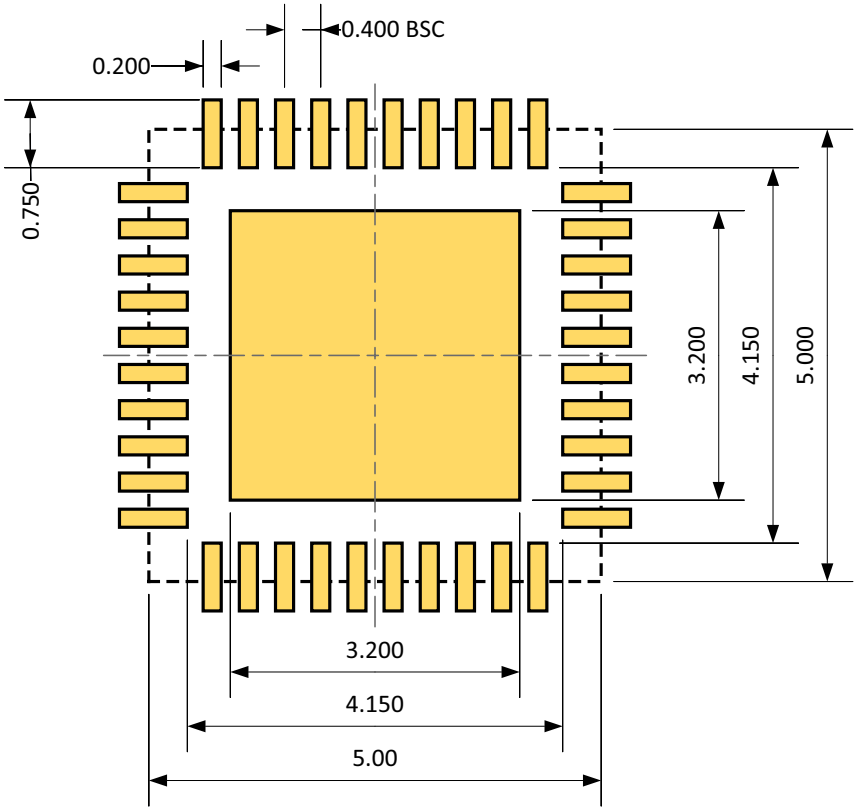

Figure 19: Recommended Board Layout for QFN40 package (All Dimensions in mm)

13. Revision History

Revision	Date	Description
0.0	January, 2021	Creation of the document. Preliminary version.
1.0	June, 2021	First version of the document
1.1	August, 2021	Minor modifications

Table 13: Revision History

