Highly efficient, regulated dual-output, ambient energy manager for Source Voltage Level Configuration with optional primary battery

Features

Ultra-low power start-up:

- Cold start from 380 mV input voltage and 3 µW input power (typical)

Constant input voltage regulation:

- Optimized for intermittent and pulse power
- Selectable operating input voltage from 50 mV to 4.5V
- Up to 110 mA current extracted from the harvester

Integrated 1.2 V/1.8 V LDO regulator:

- Up to 20 mA load current
- Power gated dynamically by external control
- Selectable output voltage

Integrated 1.8 V - 4.1 V LDO regulator

- Up to 80 mA load current with 300 mV drop-out
- Power gated dynamically by external control
- Selectable or adjustable output voltage

Flexible energy storage management:

- Selectable or ajustable overcharge and overdis-charge protection for any type of rechargeable battery or (super)capacitor
- Fast supercapacitor charging
- Indication when battery is running low
- Indication when output voltage regulators are available

Optional primary battery:

- Automatic switching to the primary battery when the secondary battery is exhausted

Integrated balun for dual-cell supercapacitor

Applications

- Door access systems
- Smart wearable sensors
- Smart switches home/building
- Point-of-Sales (POS)

Description

The AEM00940 is an integrated energy management circuit that extracts DC power to simultaneously store energy in a rechargeable element and supply the system with two independent regulated voltages. The AEM00940 allows to extend battery lifetime and ultimately eliminates the primary energy storage element in a large range of source such as pulse source, intermittent source, capacitive source and constant MPP source.

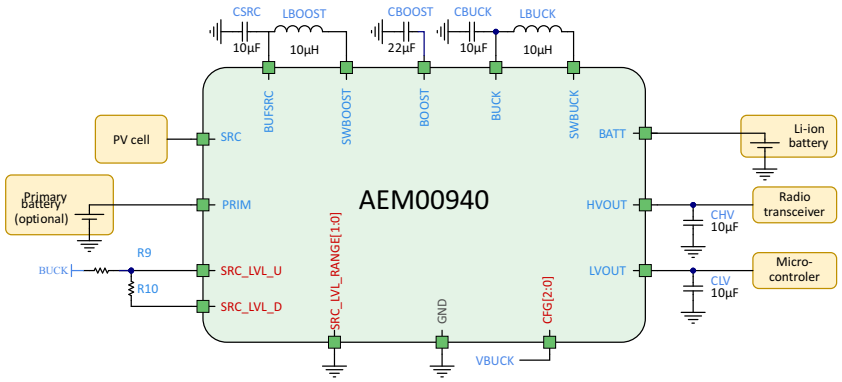
The AEM00940 harvests the available input current up to 110 mA while regulating the source at a voltage that is configured by the user. It integrates an ultra-low power boost converter to charge a storage element, such as a Li-ion battery, a thin film battery, a supercapacitor or a conventional capacitor.

Thanks to its selectable operating input voltage, it is possible to set a voltage at which the AEM00940 operates. This voltage is between 50 mV et 4.5 V. With its unique cold-start circuit, it can start operating with empty storage elements at an input voltage as low as 380 mV and an input power of just 3 µW.

The low-voltage supply typically drives a microcontroller at 1.2 V or 1.8 V. The high-voltage supply typically drives a radio transceiver at a configurable voltage between 1.8 V and 4.1 V. Both are driven by highly-efficient LDO (Low DropOut) regulators for low noise and high stability.

Configuration pins determine various operating modes by setting predefined conditions for the energy storage element (overcharge or overdischarge voltages), and by selecting the voltage of the high-voltage supply and the low-voltage supply.

The chip integrates all the active elements for powering a typical wireless sensor. Five capacitors, two inductors and two resistors are required, available in the small 0402 and 0603 size, respectively. With only seven external components, integration is maximum, footprint and BOM are minimum, optimizing the time to-market and the costs of designs.



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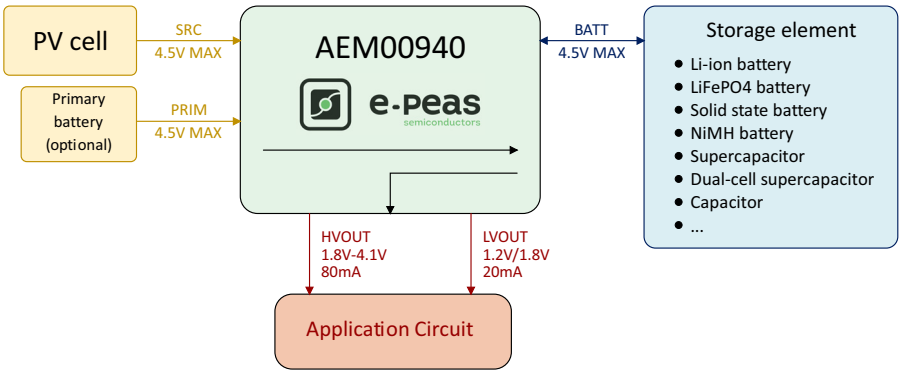


Figure 1: Simplified schematic view

1. Introduction

The AEM00940 is a full-featured energy efficient power management circuit able to charge a storage element (battery or supercapacitor, connected to BATT) from an energy source (connected to SRC) as well as to supply loads at different operating voltages through two power supplying LDO regulators (LVOUT and HVOUT).

The heart of the AEM00940 is a cascade of two regulated switching converters, namely the boost converter (See Section 10) and the buck converter with high-power conversion efficiencies.

At first start-up, as soon as a required cold-start voltage of 380 mV and a scant amount of power of just 3 µW are available from the harvested energy source, the AEM coldstarts. After the cold start, the AEM can extract the power available and regulate the source at the voltage configured by the user.

Through three configuration pins (CFG[2:0]), the user can select a specific operating mode from a range of seven modes that cover most application requirements without any dedicated external component. Those operating modes define the LDO output voltages and the protection levels of the storage element.

Depending on the harvester, the source regulation voltage, $V_{SRC,REG}$, can be configured thanks to two resistors and two configuration pins (SRC_LVL_RANGE[1:0])

Two logic control pins are provided (ENLV and ENHV) to dynamically activate or deactivate the LDO regulators that supply the low- and high-voltage load, respectively. The status pin STATUS[0] alerts the user that the LDOs are operational and can be enabled. This signal can also be used to enable an optional external regulator.

If the battery voltage gets depleted, the LDOs are power gated and the controller is no longer supplied by the storage element to protect it from further discharge. Around 600 ms before the shutdown of the AEM, the status pin STATUS[1] alerts the user for a clean shutdown of the system.

However, if the storage element gets depleted and an optional primary battery is connected on PRIM, the chip automatically uses it as a source to recharge the storage element before switching back to the ambient source. This guarantees continuous operation even under the most adverse conditions (See Section 7.4). STATUS[1] is asserted when the primary battery is providing power.

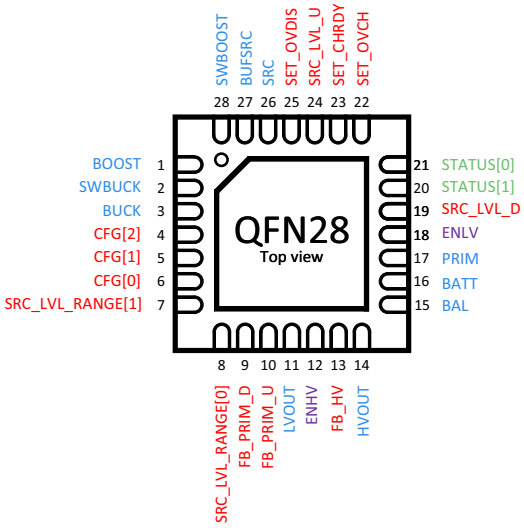


Figure 2: Pinout diagram QFN 28-pin

NAME	PIN NUMBER	FUNCTION
Power pins		
BOOST	1	Output of the boost converter.
SWBUCK	2	Switching node of the buck converter.
BUCK	3	Output of the buck converter.
LVOUT	11	Output of the low voltage LDO regulator .
HVOUT	14	Output of the high voltage LDO regulator.
BAL	15	Connection to mid-point of a dual-cell supercapapcitor (optional). Must be connected to GND if not used.
BATT	16	Connection to the energy storage element, battery or capacitor. Cannot be left floating.
PRIM	17	Connection to the primary battery (optional). Must be connected to GND if not used.
SRC	26	Connection to the harvested energy source.
BUFSRC	27	Connection to an external capacitor buffering the boost converter input.
SWBOOST	28	Switching node of the boost converter.
Configuration pins		
CFG[2]	4	Used for the configuration of the threshold voltages for the energy storage element and the output voltage of the LDOs.
CFG[1]	5	
CFG[0]	6	
SRC_LVL_RANGE[1]	7	Used for the configuration of the range for the source voltage regulation. Cannot be left floating.
SRC_LVL_RANGE[0]	8	
FB_PRIM_D	9	Used for the configuration of the primary battery (optional). Must be connected to GND if not used.
FB_PRIM_U	10	
FB_HV	13	Used for the configuration of the high-voltage LDO in the custom mode (optional). Must be left floating if not used.
SRC_LVL_D	19	Used for the configuration of the source voltage regulation. Cannot be left floating.
SRC_LVL_U	24	
SET_OVCH	22	Used for the configuration of the threshold voltages for the energy storage element in the custom mode (optional). Must be left floating if not used.
SET_CHRDY	23	
SET_OVDIS	25	

Table 1: Pins description (Part 1)

NAME	PIN NUMBER	FUNCTION	
Control pins			
ENHV	12	Enabling pin for the high-voltage LDO.	See table 8
ENLV	18	Enabling pin for the low-voltage LDO.	
Status pins			
STATUS[1]	20	Logic output. Asserted if the battery voltage falls below V_{OVDIS} or if the AEM is taking energy from the primary battery.	
STATUS[0]	21	Logic output. Asserted when the LDOs can be enabled.	
Other pins			
GND	Exposed pad	Ground connection, should be solidly tied to the PCB ground plane	

Table 2: Pins description (Part 2)

2. Absolute Maximum Ratings

Parameter	Rating
V_{SRC}	5.5 V
Operating junction temperature	- 40 °C to + 125 °C
Storage temperature	- 65 °C to + 150 °C

Table 3: Absolute maximum ratings

3. Thermal Resistance

Package	θJA	θJC	Unit
TBD	38.3	2.183	°C/W

Table 4: Thermal data

ESD CAUTION		
	ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE These devices have limited built-in ESD protection and damage may thus occur on devices subjected to high-energy ESD. Therefore, proper EESD precautions should be taken to avoid performance degradation or loss of functionality	
VESD	Human-body model according to Jedec JS001-2017	± 500 V
	Charge device model according to Jedec JS002-2014	± 1000 V

Table 5: ESD caution

4. Typical Electrical Characteristics at 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input voltage and input power						
P_{SRC_CS}	Source power required for cold start.	During cold start	3			µW
V_{SRC}	Input voltage of the energy source.	During cold start	0.38		4.5	V
		After cold start	0.05		4.5	
V_{SRC_REG}	Regulation voltage of the source		0.05		4.5	V
I_{SRC}	Input current of the energy source				110	mA
DC-DC converters						
V_{BOOST}	Output of the boost converter.	During normal operation	2.2		4.5	V
V_{BUCK}	Output of the buck converter.	During normal operation	2	2.2	2.5	
Storage element						
V_{BATT}	Voltage on the storage element.	Storage element is a rechargeable battery	2.2		4.5	V
		Storage element is a capacitor	0		4.5	V
T_{crit}	Time before shutdown once STATUS[1] has been asserted.		400	600	800	ms
V_{PRIM}	Voltage on the primary battery.		0.6		4.5	V
I_{prim}	Current from the primary battery.			20		mA
$V_{FB\_PRIM\_U}$	Feedback for the minimal voltage level on the primary battery		0.15		1.1	V
$V_{SRC\_LVL\_U}$	Voltage on the SRC_LVL_U pin		0		1.35	V
V_{OVCH}	Maximum voltage accepted on the storage element before disabling the boost converter.	see Table 9	2.3		4.5	V
V_{CHRDY}	Minimum voltage required on the storage element before enabling the LDOs after a cold start.	see Table 9	2.25		4.45	V
V_{OVDIS}	Minimum voltage accepted on the storage element before switching to primary battery or entering into a shutdown.	see Table 9	2.2		4.4	V
Low-Voltage LDO regulator						
V_{LV}	Output voltage of the low-voltage LDO.	see Table 9	1.2		1.8	V
I_{lv}	Load current from the low-voltage LDO.		0		20	mA
V_{HV}	Output voltage of the high-voltage LDO.	see Table 9	1.8		V_{batt} - 0.3	V
I_{hv}	Load current from the high-voltage LDO.		0		80	mA
STATUS[1:0]	Logic output levels on the status pins.	Logic high (VOH)	1.98	V_{BATT}		V
		Logic Low (VOL)	-0.1		0.1	V

Table 6: Electrical characteristics

5. Recommended Operation Conditions

Symbol	Parameter		Min	Typ	Max	Unit
CSRC	Capacitor decoupling the BUFSRC pin.		8	10		µF
CBOOST	Capacitor of the boost converter.		10	22	25	µF
LBOOST	Inductor of the boost converter.		4	10	25	µF
CBUCK	Capacitor of the buck converter		8	10	22	µF
LBUCK	Inductor of the buck converter		4	10	25	µF
CLV	Capacitor decoupling the low-voltage LDO regulator.		8	10	14	µF
CHV	Capacitor decoupling the high-voltage LDO regulator.		8	10	14	µF
CBATT	**Optional** - Capacitor on BATT if no storage element is connected (see Section 8.4).		150			µF
RT	**Optional** - Resistor for setting threshold voltage of the battery in custom mode. Equal to R1 + R2 + R3 + R4 (see Section 8.1.1).		1	10	100	MΩ
RV	**Optional** - Resistor for setting the output voltage of the high-voltage LDO in custom mode. Equal to R5 + R6 (see Section 8.1.1).		1	10	40	MΩ
RP	**Optional** - Resistor to be used with a primary battery. Equal to R7 + R8 (see Section 8.3).		100		500	kΩ
RS	Resistor to be used for the source voltage regulation Equal to R9 + R10 (see Section 8.2).		0.1		1	MΩ
ENHV	Enabling pin for the high-voltage LDO[1].	Logic high (VOH)	1.75	V_{BUCK}	V_{BUCK}	V
		Logic low (VOL)	-0.01	0	0.01	
ENLV	Enabling pin for the low-voltage LDO[2].	Logic high (VOH)	1.75	V_{BUCK}	V_{BOOST}	V
		Logic low (VOL)	-0.01	0	0.01	
CFG[2:0]	Configuration pins for the storage element (see Table 9).	Logic high (VOH)	Connect to BUCK			
		Logic low (VOL)	Connect to GND			
SRC_LVL_RANGE[1:0]	Configuration pins for the range of the source voltage regulation configuration	Logic high (VOH)	Connect to BUCK			
		Logic low (VOL)	Connect to GND			

Table 7: Recommended operating conditions

1. ENHV can be dynamically driven by a logic signal from the LV domain. For a static usage, connect to BUCK (High) or GND (Low).
2. ENLV can be dynamically driven by a logic signal from the HV domain. For a static usage, connect to BUCK or BOOST (High) or GND (Low).

6. Functional Block Diagram

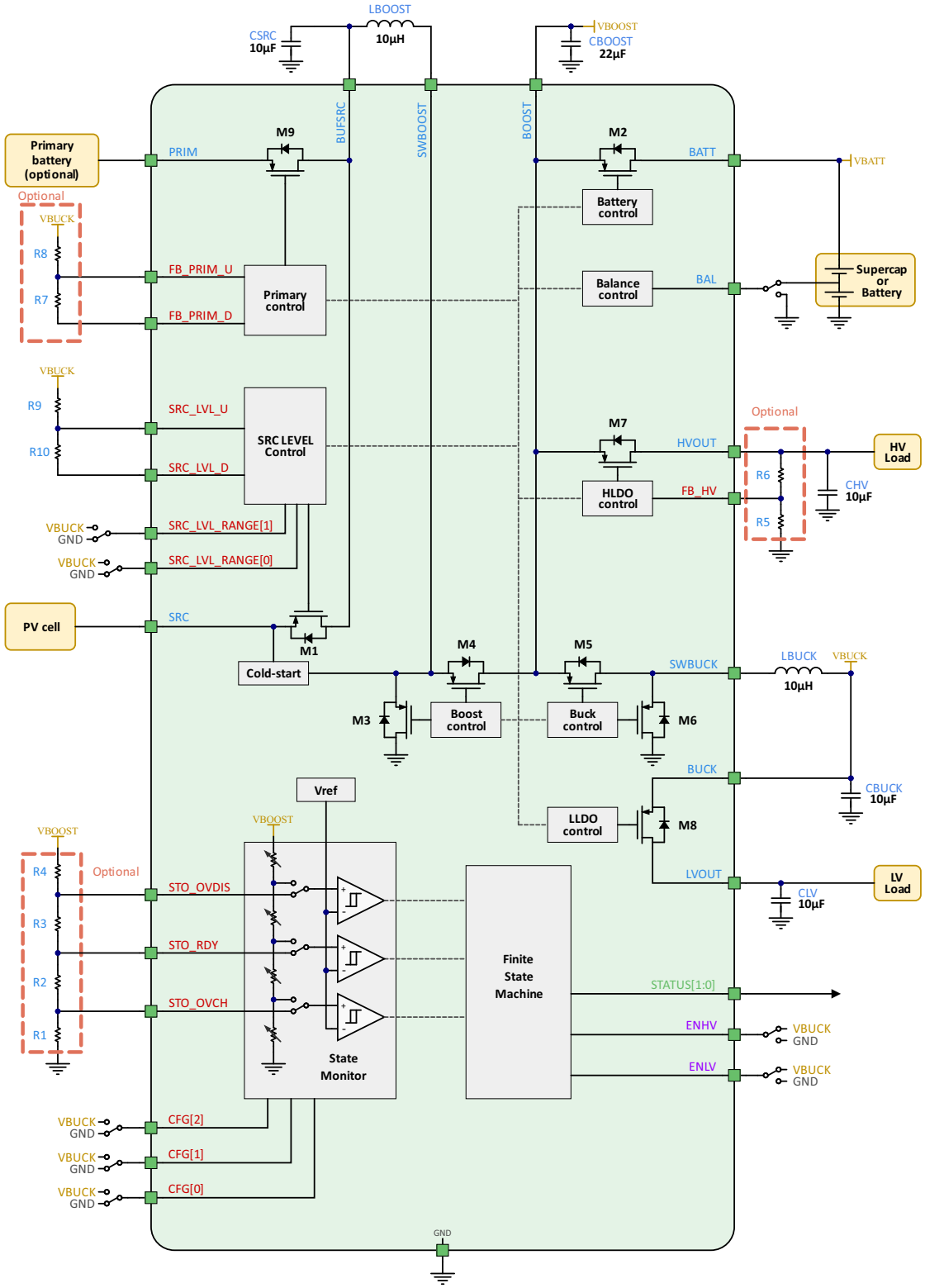


Figure 3: Functional block diagram

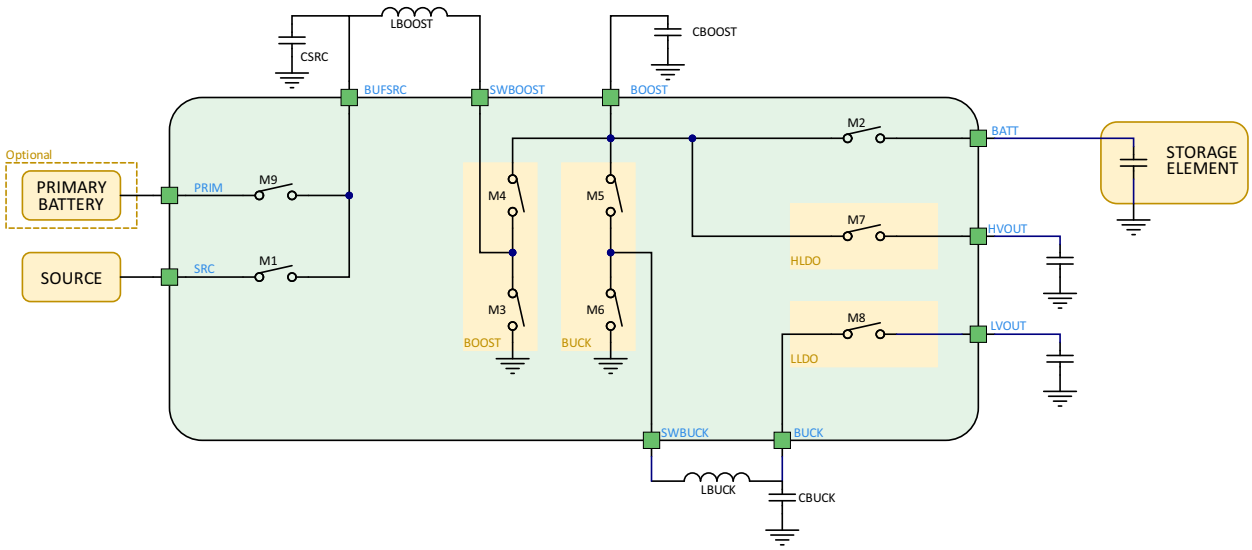


Figure 4: Simplified schematic view of the AEM00940

7. Theory of Operation

7.1. Deep sleep & Wake up modes

The DEEP SLEEP MODE is a state where all nodes are deeply discharged and there is no available energy to be harvested. As soon as the required cold-start voltage of 380 mV and a sparse amount of power of just 3 µW becomes available on SRC, the WAKE-UP MODE is activated. V_{BOOST} and V_{BUCK} rises up to a voltage of 2.2 V. V_{BOOST} then rises alone up to V_{OVCH}.

At that stage, both LDOs are internally deactivated. Therefore, STATUS[0] is equal to 0 as shown in Figure 9 and Figure 10. When V_{BOOST} reaches V_{OVCH}, two scenarios are possible: in the first scenario, a super-capacitor or a capacitor having a voltage lower than V_{CHRDY} is connected to the BATT node. In the second scenario, a charged battery is connected to the BATT node.

7.1.1. Supercapacitor as a storage element.

If the storage element is a supercapacitor, the storage element may need to be charged from 0 V. The boost converter charges BATT from the input source and by modulating the conductance of M2. During the charge of the BATT node, both LDOs are deactivated and STATUS[0] is de-asserted. When V_{BATT} reaches V_{CHRDY}, the circuit enters NORMAL MODE, STATUS[0] is asserted and the LDOs can be activated by the user using the ENLV and ENHV control pins as shown in Figure 9.

7.1.2. Battery as a storage element.

If the storage element is a battery, but its voltage is lower than V_{CHRDY}, then the storage element first needs to be charged until it reaches V_{CHRDY}. Once V_{BATT} exceeds V_{CHRDY}, or if the battery was initially charged above V_{CHRDY}, the circuit enters NORMAL MODE. STATUS[0] is asserted and the LDOs can be activated by the user thanks to ENLV and ENHV as shown in Figure 10.

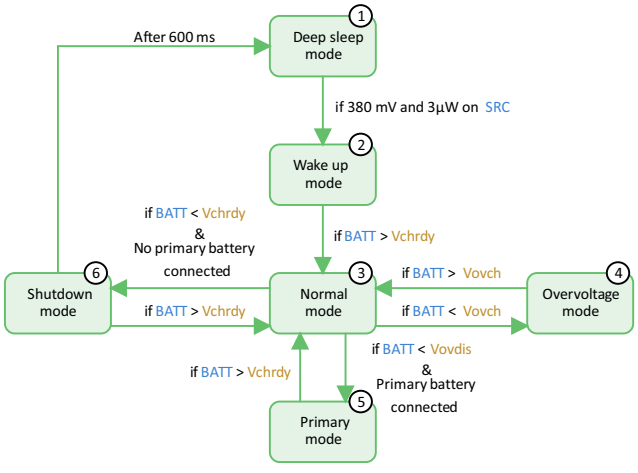


Figure 5: Diagram of the AEM00940 modes

7.2. Normal mode

Once the AEM enters NORMAL MODE, three scenarios are possible:

- There is enough power provided by the source to maintain V_{BATT} above V_{OVDIS} but V_{BATT} is below V_{OVCH}. In that case, the circuit remains in NORMAL MODE.
- The source provides more power than the load consumes and V_{BATT} increases above V_{OVCH}, the circuit enters OVERVOLTAGE MODE, as explained in Section 7.3.
- Due to a lack of power from the source, V_{BATT} falls below V_{OVDIS}. In this case, either the circuit enters SHUTDOWN MODE as explained in Section 7.5 or, if a charged primary battery is connected on PRIM, the circuit enters PRIMARY BATTERY MODE as explained in Section 7.4.

7.2.1. Boost

The boost (or step-up) converter raises the voltage available at BUFSRC to a level suitable for charging the storage element, in the range of 2.2 V to 4.5 V, according to the system configuration. This voltage (V_{BOOST}) is available at the BOOST pin. The switching transistors of the boost converter are M3 and M4, with the switching node available externally at SWBOOST. The reactive power components of this converter are the external inductor and capacitor LBOOST and CBOOST. Periodically, the MPP control circuit disconnects the source from the BUFSRC pin with the transistor M1 in order to measure the voltage present on SRC_LVL_U and define the source regulation voltage. BUFSRC is decoupled by the capacitor CSRC, which smooths the voltage against the current pulses induced by the boost converter.

The storage element is connected to the BATT pin, at a voltage V_{BATT}. This node is linked to BOOST through the transistor M2. In NORMAL MODE, this transistor effectively shorts the battery to the BOOST node ($V_{BATT} = V_{BOOST}$). When energy harvesting is occurring, the boost converter delivers a current that is shared between the battery and the loads. M2 is opened to disconnect the storage element when V_{BATT} reaches V_{OVDIS}. However, in such a scenario, the AEM00940 offers the possibility of connecting a primary battery to recharge V_{BATT} up to the V_{CHRDY}. The transistor M9 connects PRIM to BUFSRC and the transistor M1 is opened to disconnect the SRC input pin as explained in the PRIMARY BATTERY MODE section.

7.2.2. Buck

The buck (or step-down) converter lowers the voltage from V_{BOOST} to a constant V_{BUCK} value of 2.2 V. This voltage is available at the BUCK pin. The switching transistors of the buck converter are M5 and M6, with the switching node available externally at SWBUCK. The reactive power components of the buck converter are the external inductor LBUCK and the capacitor CBUCK.

7.2.3. LDO outputs

Two LDOs are available to supply loads at different operating voltages:

Through M7, V_{BOOST} supplies the high-voltage LDO that powers its load through HVOUT. This regulator delivers a clean voltage (V_{HV}) with a maximum current of 80 mA on HVOUT. In the built-in configuration modes, an output voltage of 1.8 V, 2.5 V or 3.3 V can be selected. In the custom configuration mode, it is adjustable between 1.8 V and V_{BATT} - 0.3 V.The high-voltage output can be dynamically enabled or disabled with the logic control pin ENHV. The output is decoupled by the external capacitor CHV.

Through M8, V_{BUCK} supplies the low-voltage LDO that powers its load through LVOUT. This regulator delivers a clean voltage (V_{LV}) of 1.8 V or 1.2 V with a maximum current of 20 mA on LVOUT. The low-voltage output can be dynamically enabled or disabled with the logic control pin ENLV. The output is decoupled by the external capacitor CLV.

Status pin STATUS[0] alerts the user when the LDOs can be enabled as explained in the DEEP SLEEP MODE & WAKE-UP MODE section and in the SHUTDOWN MODE section. The table below shows the four possible configurations:

ENLV	ENHV	LV output	HV output
1	1	Enabled	Enabled
1	0	Enabled	Disabled
0	1	Disabled	Enabled
0	0	Disabled	Disabled

Table 8: LDOs configurations

7.3. Overcharge mode

When V_{BATT} reaches V_{OVCH}, the charge is complete and the internal logic maintains V_{BATT} around V_{OVCH} with a hysteresis of a few mV as shown in Figure 11 to prevent damage to the storage element and to the internal circuitry. In this configuration, the boost converter is periodically activated to maintain V_{BATT} and the LDOs are still available. Moreover, when the boost converter is not activated, the transistor M1 in Figure 4 is opened to prevent current from the source to the storage element when V_{SRC} is higher than V_{OVCH}.

7.4. Primary mode

When V_{BATT} drops below V_{OVDIS}, the circuit compares the voltage on PRIM with the voltage on FB_PRIM_U to determine whether a charged primary battery is connected on PRIM. The voltage on FB_PRIM_U is set thanks to two optional resistances as explained in the Primary battery configuration section. If the voltage on PRIM divided by 4 is higher than the voltage on FB_PRIM_U, the circuit considers the primary battery as available and the circuit enters PRIMARY BATTERY MODE.

In that mode, transistor M1 is opened and the primary battery is connected to BUFSRC through transistor M9 to become the source of energy for the AEM00940. The chip remains in this mode until V_{BATT} reaches V_{CHRDY}. When V_{BATT} reaches V_{CHRDY}, the circuit enters NORMAL MODE. As long as the chip is in PRIMARY BATTERY MODE, STATUS[1] is asserted.

If no primary battery is used in the application, PRIM, FB_PRIM_U and FB_PRIM_D must be tied to GND.

7.5. Shutdown mode

When V_{BATT} drops below V_{OVDIS} and no power is available from a primary battery, the circuit enters SHUTDOWN MODE as shown in Figure 5 to prevent deep discharge potentially leading to damage to the storage element and instability of the LDOs. The circuit asserts STATUS[1] to warn the system that a shutdown will occur. Both LDO regulators remain enabled.

If no primary battery is used, this allows the load, whether it is powered on LVOUT or HVOUT, to be interrupted by the low to-high transition of STATUS[1], and to take all appropriate actions before power shutdown.

If V_{BATT} recovers to V_{CHRDY} within T_{crit} (~600 ms), the AEM returns in NORMAL MODE. But if, after T_{crit}, V_{BATT} does not reach V_{CHRDY}, the circuit enters DEEP SLEEP MODE. The LDOs are deactivated and BATT is disconnected from BOOST to avoid damaging the battery due to the overdischarge. From now, the AEM will have to go through the wake-up procedure described in the DEEP SLEEP MODE & WAKE-UP MODE section.

7.6. Balun for dual-cell supercapacitor

The balun circuit allows users to balance the internal voltage in a dual-cell supercapacitor in order to avoid damaging the super-capacitor because of excessive voltage on one cell. If BAL is connected to GND, the balun circuit is disabled. This configuration must be used if a battery, a capacitor or a single-cell supercapacitor is connected on BATT. If BAL is connected to the node between the cells of a supercapacitor, the balun circuit compensates for any mismatch of the two cells that could lead to over-charge of one of both cells. The balun circuit ensures that BAL remains close to $V_{BATT}/2$. This configuration must be used if a dual-cell supercapacitor is connected on BATT.

8. System configuration

Configurations pins			Storage element threshold voltages			LDOs output voltages		Typical use
CFG[2]	CFG[1]	CFG[0]	V_{OVCH}	V_{CHRDY}	V_{OVDIS}	V_{HV}	V_{LV}	
1	1	1	4.12 V	3.67 V	3.60 V	3.3 V	1.8 V	Li-ion battery
1	1	0	4.12 V	4.04 V	3.60 V	3.3 V	1.8 V	Solid state battery
1	0	1	4.12 V	3.67 V	3.01 V	2.5 V	1.8 V	Li-ion/NiMH battery
1	0	0	2.70 V	2.30 V	2.20 V	1.8V	1.2 V	Single-cell supercapacitor
0	1	1	4.50 V	3.67 V	2.80 V	2.5 V	1.8 V	Dual-cell supercapacitor
0	1	0	4.50 V	3.92 V	3.60 V	3.3 V	1.8 V	Dual-cell supercapacitor
0	0	1	3.63 V	3.10 V	2.80 V	2.5 V	1.8 V	LiFePO4 battery
0	0	0	Custom mode - Programmable through R1 to R6				1.8 V	

Table 9: Usage of CFG[2:0]

8.1. Battery and LDOs configuration

Through three configuration pins (CFG[2:0]), the user can set a particular operating mode from a range that covers most application requirements, without any dedicated external component as shown in Table 9. The three threshold levels are defined as:

- V_{OVCH}: Maximum voltage accepted on the storage element before disabling the boost converter,
- V_{CHRDY}: Minimum voltage required on the storage element after a cold start before enabling the LDOs,
- V_{OVDIS}: Minimum voltage accepted on the storage element before considering the storage element as depleted.

See Theory of Operation section for more information about the purposes of these thresholds.

The two LDOs output voltages are called V_{HV} and V_{LV} for the high- and low-output voltages, respectively. In the built-in configuration mode, seven combinations of these voltage levels are hard-wired and selectable through the CFG[2:0] configuration pins, covering most application cases.

8.1.1. Custom mode

When CFG[2:0] are tied to GND, the custom mode is selected and all six configuration resistors shown in Figure 6, must be wired as follows:

V_{OVCH}, V_{CHRDY} and, V_{OVDIS} are defined thanks to R1, R2, R3 and R4. If we define the total resistor (R1 + R2 + R3 + R4) as RT, R1, R2, R3 and R4 are calculated as:

- $1M\Omega \leq RT \leq 100M\Omega$
- $R1 = RT \cdot \frac{1V}{V_{OVCH}}$
- $R2 = RT \cdot \left(\frac{1V}{V_{CHRDY}} - \frac{1V}{V_{OVCH}}\right)$
- $R3 = RT \cdot \left(\frac{1V}{V_{OVDIS}} - \frac{1V}{V_{CHRDY}}\right)$
- $R4 = RT \cdot \left(1 - \frac{1V}{V_{OVDIS}}\right)$

V_{HV} is defined thanks to R5 and R6. If we define the total resistor (R5 + R6) as RV, R5 and R6 are calculated as:

- $1M\Omega \leq RV \leq 40M\Omega$
- $R5 = RV \cdot \frac{1V}{V_{HV}}$
- $R6 = RV \cdot \left(1 - \frac{1V}{V_{HV}}\right)$

The resistors should have high values to make the additional power consumption negligible. Moreover, the following constraints must be adhered to ensure the functionality of the chip:

- $V_{CHRDY} + 0{,}05V \leq V_{OVDIS} \leq 4{,}5V$
- $V_{OVDIS} + 0{,}05V \leq V_{CHRDY} \leq V_{OVCH} - 0{,}5V$
- $2{,}2V \leq V_{OVDIS}$
- $V_{HV} \leq V_{OVDIS} - 0{,}3V$

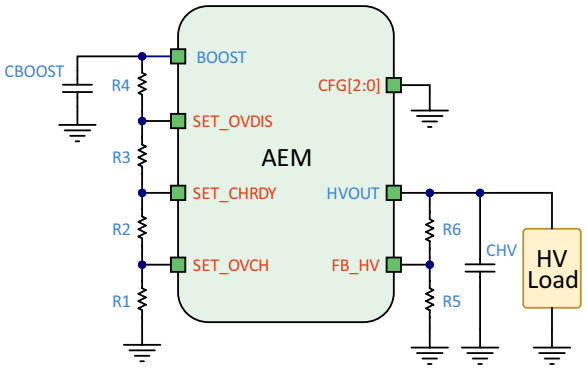


Figure 6: Custom configuration resistors

8.2. Source voltage configuration

The source voltage regulation is set thanks to two resistors and two configuration pins. During the evaluation of V_{SRC_REG}, the circuit connects SRC_LVL_D to GND and measures the voltage present on SRC_LVL_U and multiply by the gain set by SRC_LVL_RANGE[1:0].

If we define the total resistor (R9 + R10) as RS, R9 and R10 are calculated as:

- $100k\Omega \leq RS \leq 1M\Omega$
- $V_{SRC\_LVL\_U} = \frac{V_{SRC\_REG}}{GAIN}$
- $R10 = \frac{V_{SRC\_REG}}{Gain} \cdot RS \cdot \frac{1}{2,2V}$
- $R9 = RS - R10$

The table below shows the different ranges accessible for the different configuration.

Configuration pins		
SRC_LVL_RANGE[1:0]	Gain	Range for V_{SRC_REG}
00	x1	lower than 1.35V
01	x2	Between 1.35 V and 2.7 V
10	x4	Between 2.7 V and 4.47 V
11		

Table 10: SRC_LVL_RANGE[1:0] configuration

8.3. Primary battery configuration

To use the primary battery, it is mandatory to determine $V_{PRIM,MIN}$, the voltage of the primary battery at which it has to be considered as empty. During the evaluation of $V_{PRIM,MIN}$, the circuit connects FB_PRIM_D to GND. The circuit uses a resistive divider between BUCK and FB_PRIM_D to define the voltage on FB_PRIM_U as $V_{PRIM,MIN}$ divided by 4.

When $V_{PRIM,MIN}$ is not evaluated, FB_PRIM_D is left floating to avoid quiescent current on the resistive divider. If we define the total resistor (R7 + R8) as RP, R7 and R8 are calculated as:

- $100k\Omega \leq RP \leq 500k\Omega$
- $R7 = \frac{V_{PRIM\_MIN}}{4} \cdot RP \cdot \frac{1}{2,2V}$
- $R8 = RP - R7$

Note that FB_PRIM_U, FB_PRIM_D and PRIM must be tied to GND if no primary battery is used.

8.4. No-battery configuration

If the harvested energy source is permanently available and covers the application purposes or if the application does not need to store energy when the harvested energy source is not available, the storage element may be replaced by an external capacitor CBATT of minimum 150 µF.

8.5. Storage element information

The energy storage element of the AEM00940 can be a rechargeable battery, a supercapacitor or a large capacitor (minimum 150 µF). It should be chosen so that its voltage does not fall below V_{OVDIS} even during occasional peaks of the load current. If the internal resistance of the storage element cannot sustain this voltage limit, it is advisable to buffer the battery with a capacitor.

The BATT pin that connects the storage element must never be left floating. If the application expects a disconnection of the battery (e.g. because of a user removable connector), the PCB should include a capacitor of at least 150 µF. The leakage current of the storage element should be small as leakage currents directly impact the quiescent current of the subsystem.

8.6. External inductors information

The AEM00940 operates with two standard miniature inductors of 10 µH. LBOOST and LBUCK must respectively sustain a peak current of at least 250 mA and 50 mA and a switching frequency of at least 10 MHz. Low equivalent series resistance (ESR) favors the power conversion efficiency of the boost and buck converters.

8.7. External capacitors information

The AEM00940 operates with four identical standard miniature ceramic capacitors of 10 µF and one miniature ceramic capacitor of 22 µF. The leakage current of the capacitors should be small as leakage currents directly impact the quiescent current of the subsystem.

CSRC

This capacitor acts as an energy buffer at the input of the boost converter. It prevents large voltage fluctuations when the boost converter is switching. The recommended value is 10 µF +/- 20%.

CBUCK

This capacitor acts as an energy buffer for the buck converter. It also reduces the voltage ripple induced by the current pulses inherent to the switched mode of the converter. The recommended value is 10 µF +/- 20 %.

CBOOST

This capacitor acts as an energy buffer for the boost converter. It also reduces the voltage ripple induced by the current pulses inherent to the switched mode of the converter. The recommended value is 22 µF +/- 20%.

CHV and CLV

These capacitors ensure a high-efficiency load regulation of the high-voltage and low-voltage LDO regulators. Closed-loop stability requires the value to be in the range of 8 µF to 14 µF.

9. Typical Application Circuits

9.1. Example circuit 1

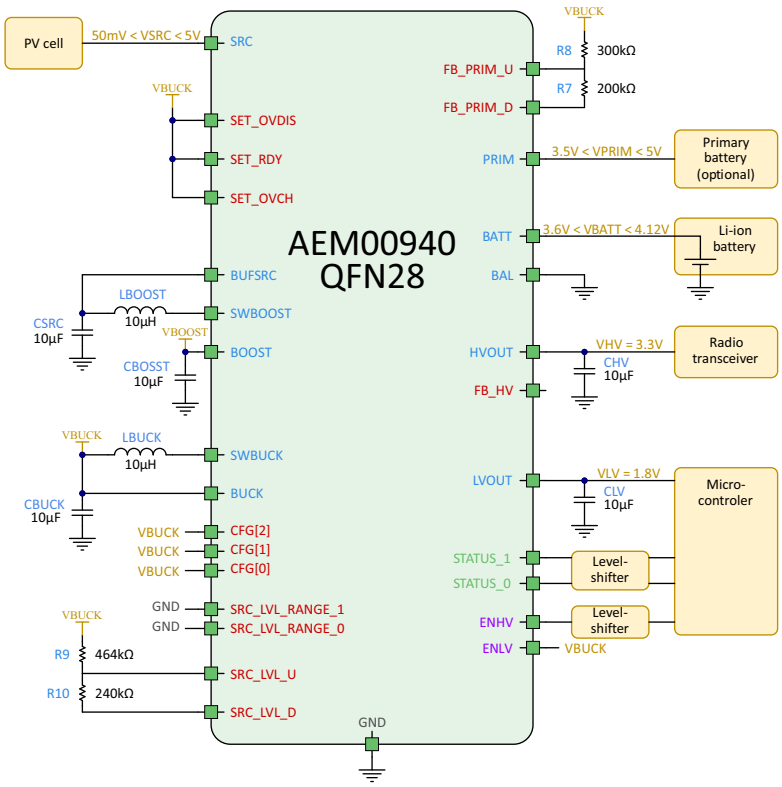


Figure 7: Typical application circuit 1

The energy source is a PV cell, and the storage element is a standard Li-ion battery cell. The radio communication makes use of a transceiver that operates from a 3.3 V supply. A micro-controller supplied by a 1.8 V supply controls the application.

This circuit uses a pre-defined operating mode, typical of systems that use standard components for radio and energy storage.

The operating mode pins are connected to:

- CFG[2:0] = 111

Referring to Table 9, in this mode, the threshold voltages are:

- V_{OVCH} = 4.12 V
- V_{CHRDY} = 3.67 V
- V_{OVDIS} = 3.60 V

Moreover, the LDOs output voltages are:

- V_{HV} = 3.3 V
- V_{LV} = 1.8 V

A primary battery is also connected as a back-up solution. The minimal level allowed on this battery is set at 3.5 V. Following equations on Section 8.3:

- $RP = 0{,}5M\Omega$
- $R7 = \frac{3{,}5V}{4} \cdot 0{,}5M\Omega \cdot \frac{1}{2{,}2V} = 200k\Omega$
- $R8 = 0{,}5M\Omega - 200k\Omega = 300k\Omega$

The PV cell used needs a constant source voltage regulation at 0.75V to extract the maximum power regardless of the brightness. SRC_LVL_RANGE[1:0] is set to 00 according to the table 10.

- $RS = 704k\Omega$
- $R10 = \frac{0{,}75}{1} \cdot 704k\Omega \cdot \frac{1}{2{,}2V} = 240k\Omega$
- $R9 = 704k\Omega - 240k\Omega = 464k\Omega$

The ENLV enable pin for the low-voltage LDO is tied to BUCK.

The microcontroller will be enabled when V_{BATT} and V_{BOOST} exceed V_{CHRDY} as the low-voltage regulator supplies it.

The application software can enable or disable the radio transceiver with a GPIO connected to ENHV.

9.2. Example circuit 2

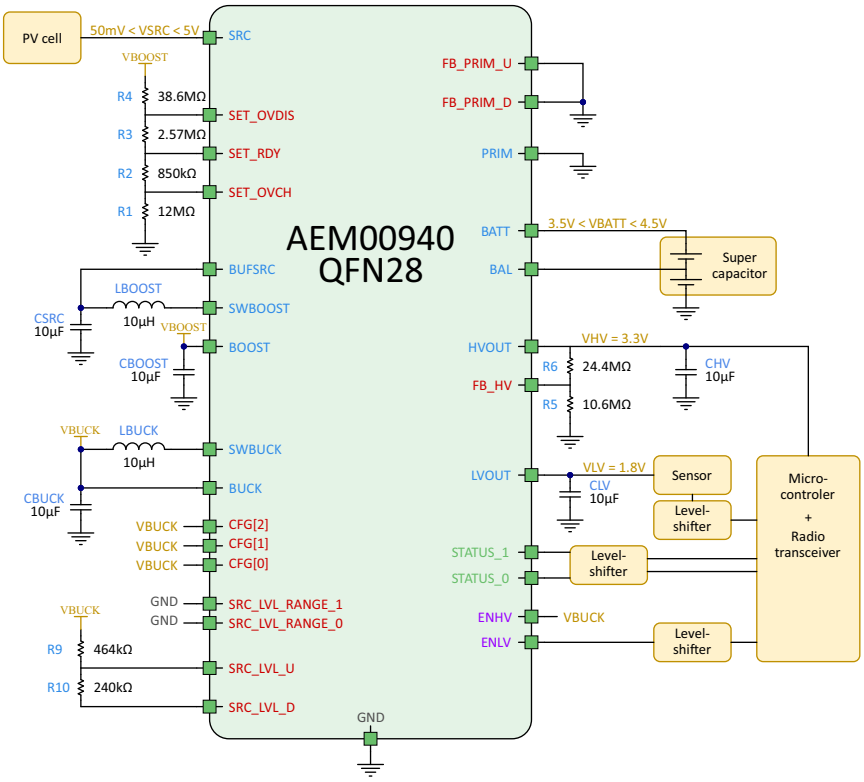


Figure 8: Typical application circuit 2

The energy source is a PV cell, and the storage element is a dual-cell supercapacitor. The supercapacitor can be completely depleted during the cold start.

Moreover, BAL is connected to the dual-cell supercapacitor to compensate for any mismatch between the two cells and in that way protect the supercapacitor.

A micro-controller pilots and collects information from a sensor. The operating mode pins are connected to:

- CFG[2:0] = 000

The user wants a custom configuration with V_{OVCH}, V_{CHRDY} and V_{OVDIS} at 4.5 V, 4.2 V and 3.5 V, respectively. The user choose 54 MΩ for RT. Following the equation on Section 8.1.1:

- $R1 = 54M\Omega \cdot \frac{1V}{4,5V} = 12M\Omega$
- $R2 = 54M\Omega \cdot \left(\frac{1V}{4,2V} - \frac{1V}{4,5V}\right) = 850k\Omega$
- $R3 = 54M\Omega \cdot \left(\frac{1V}{3,5V} - \frac{1V}{4,2V}\right) = 2,57M\Omega$
- $R4 = 54M\Omega \cdot \left(1 - \frac{1V}{3,5V}\right) = 38,6M\Omega$

In the custom mode, the V_{LV} equals 1.8 V and the application software can enable or disable the sensor with a GPIO connected to ENLV.

On V_{HV}, the user wants a 3.3 V voltage. As shown in section 8.1, the user chooses a resistor RV equal to 35 MΩ

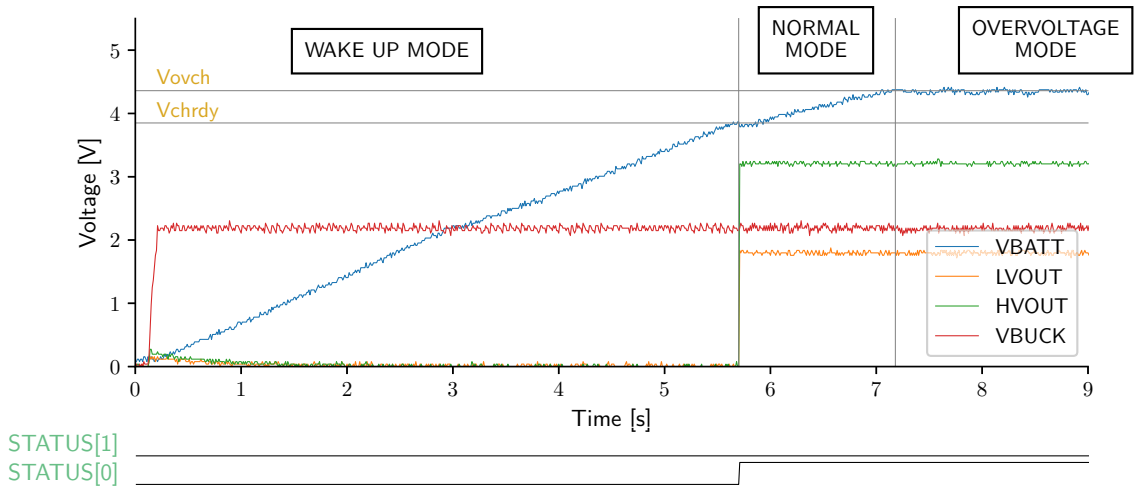
- $R5 = 35M\Omega \cdot \frac{1V}{3,3V} = 10,6M\Omega$

$R6 = 35M\Omega \cdot \left(1 - \frac{1V}{3,3V}\right) = 24,4M\Omega$ The ENHV enable pin for the high-voltage LDO is tied to BUCK. The microcontroller is enabled when V_{BATT} and V_{BOOST} exceeds V_{CHRDY} as the high-voltage regulator supplies it.

The PV cell used needs a constant source voltage regulation at 0.75V to extract the maximum power regardless of the brightness. SRC_LVL_RANGE[1:0] is set to 00 according to the table 10.

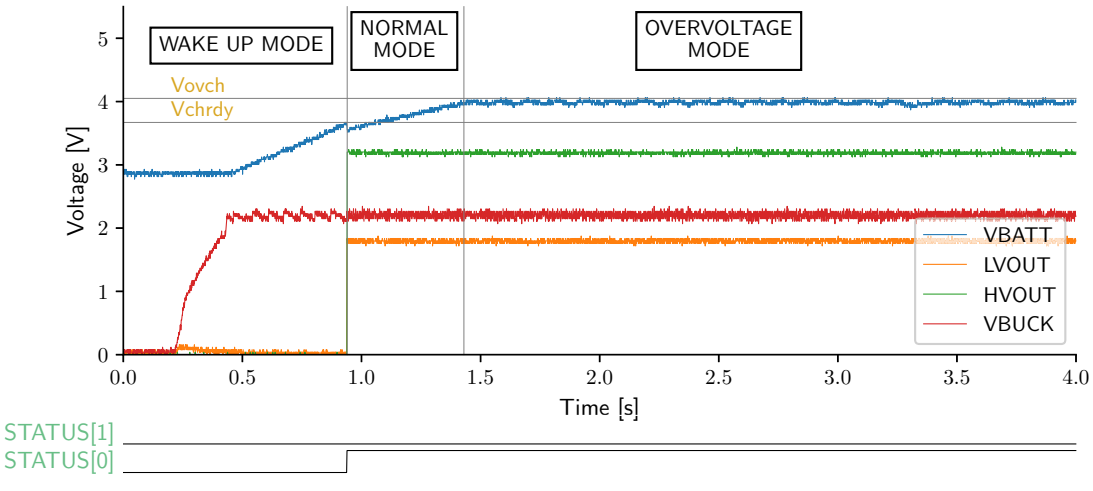
- $RS = 704k\Omega$
- $R10 = \frac{0,75}{1} \cdot 704k\Omega \cdot \frac{1}{2,2V} = 240k\Omega$
- $R9 = 704k\Omega - 240k\Omega = 464k\Omega$

No primary battery is connected and the PRIM, FB_PRIM_U and FB_PRIM_D pins are tied to GND



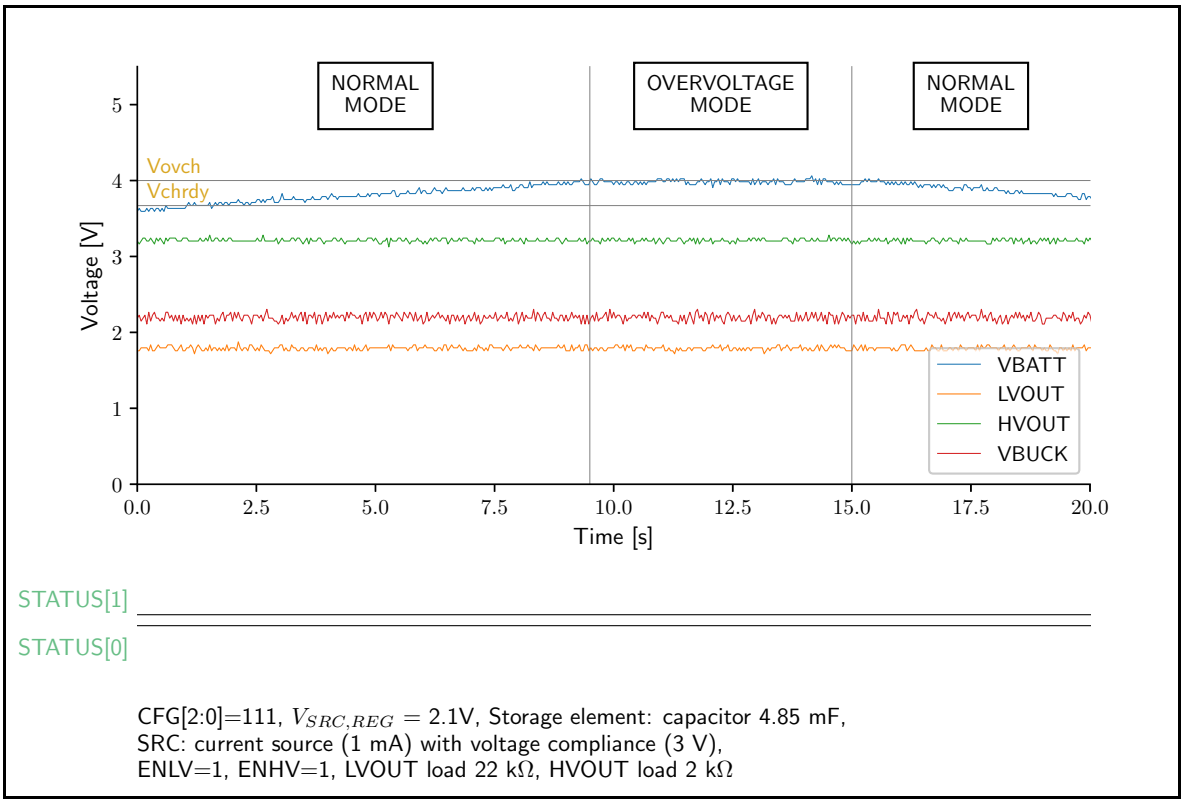
CFG[2:0]=011, $V_{SRC,REG}$ = 2.1V, Storage element: capacitor 4.85 mF,
SRC: current source (1 mA) with voltage compliance (3 V),
ENLV=1, ENHV=1, LVOUT load 22 kΩ, HVOUT load 2 kΩ

Figure 9: Cold start with a capacitor connected to BATT



CFG[2:0]=111, $V_{SRC,REG}$ = 2.1V, Storage element: capacitor 4.85 mF,
SRC: current source (1 mA) with voltage compliance (3 V),
ENLV=1, ENHV=1, LVOUT load 22 kΩ, HVOUT load 2 kΩ

Figure 10: Cold start with a battery connected to BATT



CFG[2:0]=111, $V_{SRC,REG}$ = 2.1V, Storage element: capacitor 4.85 mF,
SRC: current source (1 mA) with voltage compliance (3 V),
ENLV=1, ENHV=1, LVOUT load 22 kΩ, HVOUT load 2 kΩ

Figure 11: Overvoltage mode

10. Performance Data

10.1. BOOST conversion efficiency for LBOOST = 10 µH

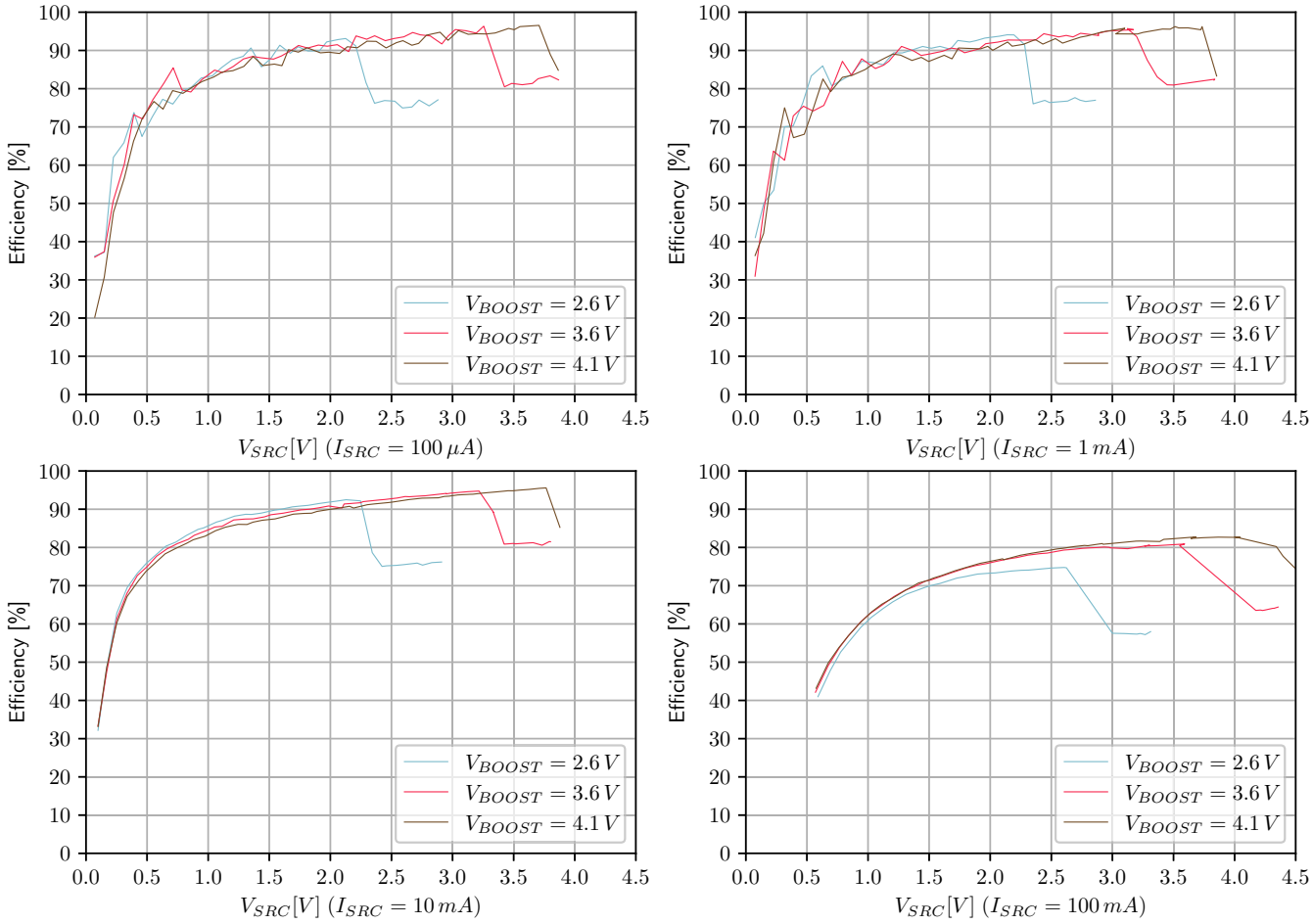


Figure 12: Boost efficiency for Isrc at 100µA, 1mA, 10mA and 100mA (LBOOST = 10 µH)

10.2. BOOST conversion efficiency for LBOOST = 22 µH

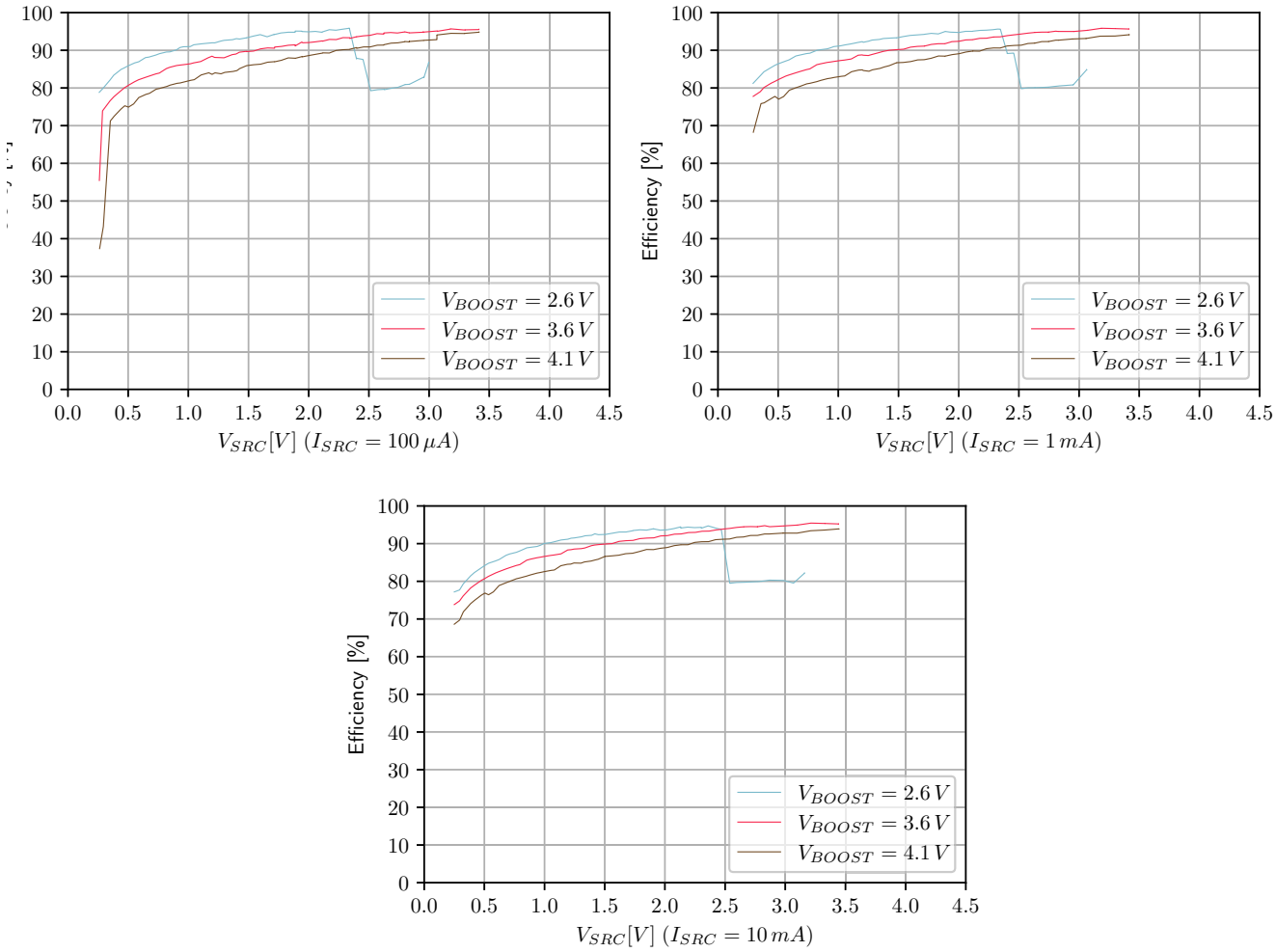


Figure 13: Boost efficiency for Isrc at 100µA, 1mA and 10mA (LBOOST = 22 µH)

10.3. Quiescent current

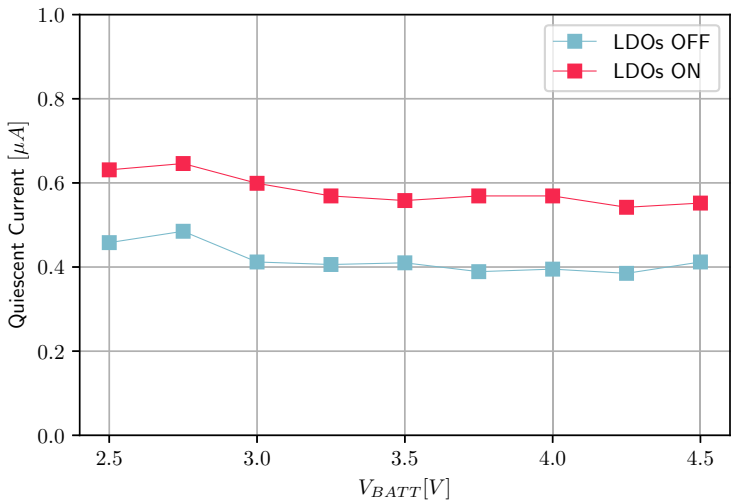


Figure 14: Quiescent current with LDOs on and off

10.4. High-voltage LDO regulation

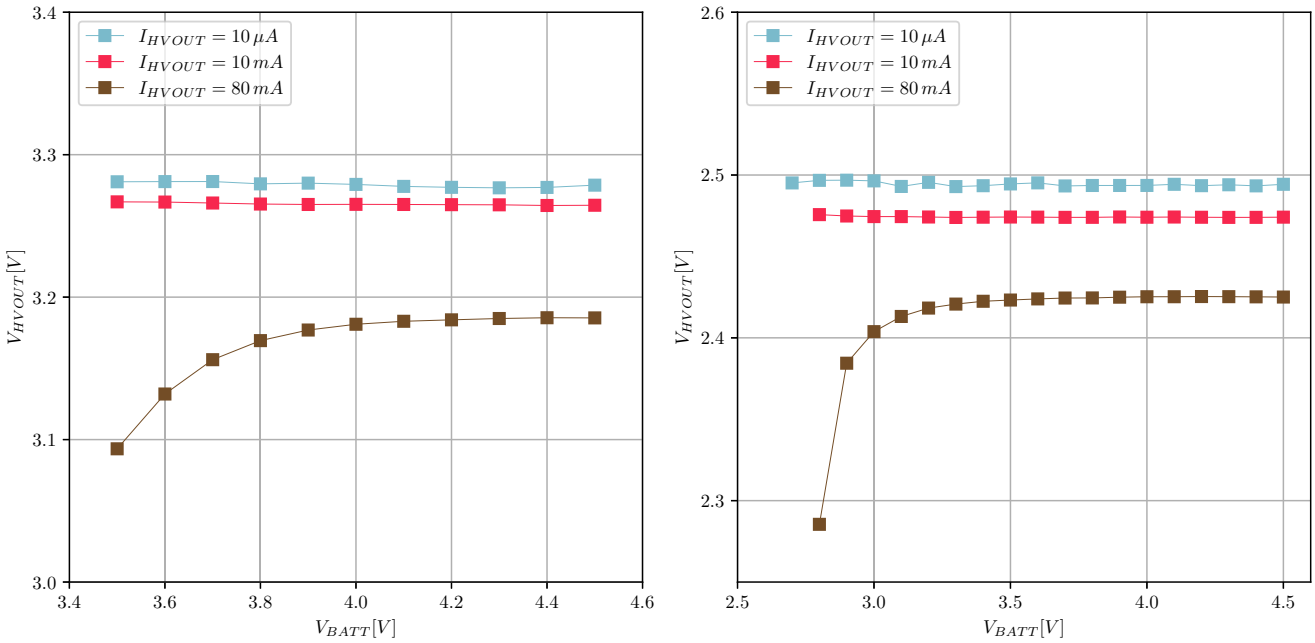


Figure 15: HVOUT at 3.3 V and 2.5 V

10.5. Low-voltage LDO regulation

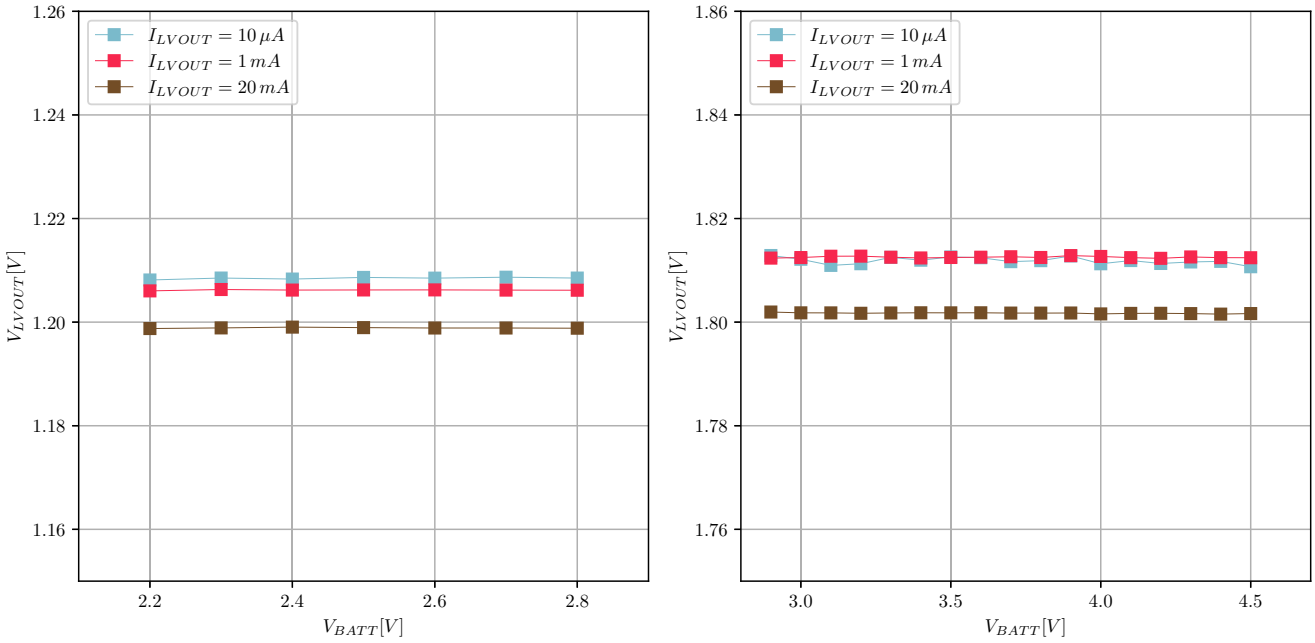


Figure 16: LVOUT at 1.2 V and 1.8 V

10.6. High-voltage LDO efficiency

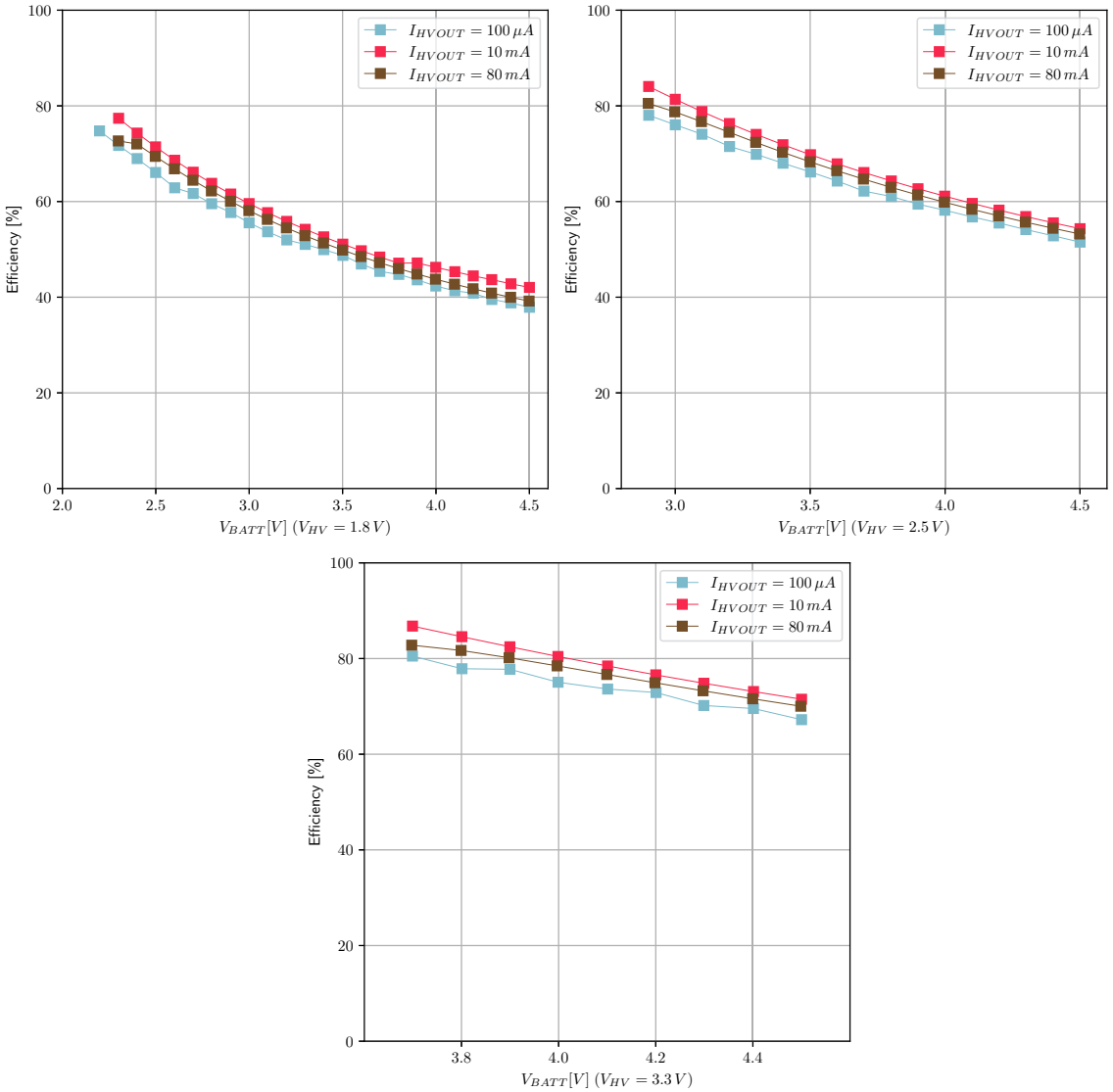


Figure 17: HVOUT efficiency at 1.8V, 2.5V and 3.3 V (values at 350 mA are from simulations)

The theoretical efficiency of a LDO can be calculated as Vout / Vin if quiescent current can be neglected with regards to the output current. In the case of the high-voltage LDO, the theoretical efficiency is equal to V_{HV} / V_{BATT}.

10.7. Low-voltage LDO efficiency

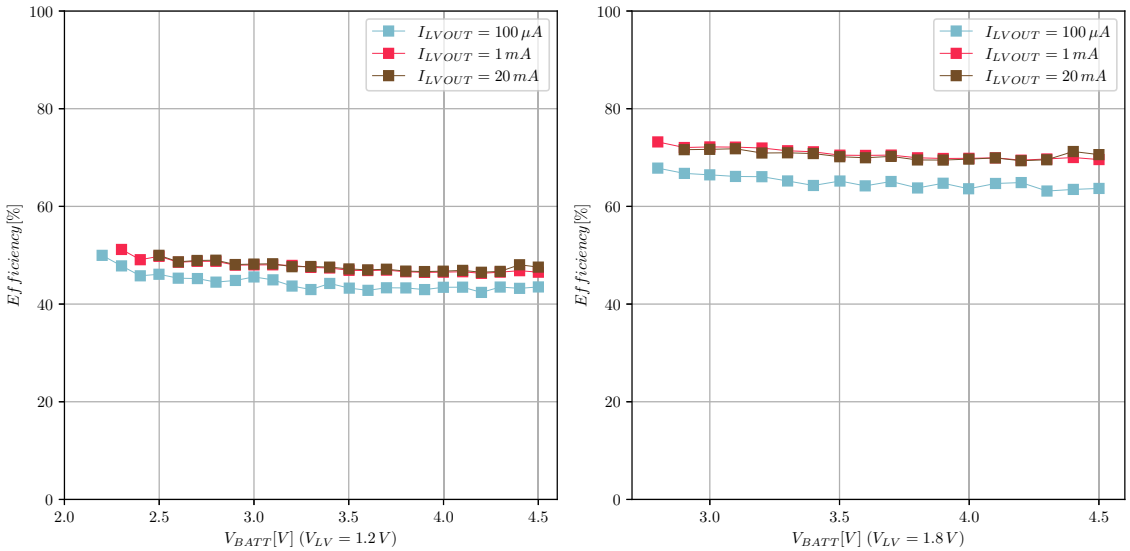


Figure 18: Efficiency of buck cascaded with LVOUT at 1.2 V and 1.8 V

The theoretical efficiency of a LDO can be calculated as V_{LV} / V_{BUCK}. Starting from the battery, the efficiency of the buck converter has to be taken into account (see Figure 4). The efficiency between V_{BATT} and V_{LV} is therefore equal to ηbuck * V_{LV} / V_{BUCK}.

11. Schematic

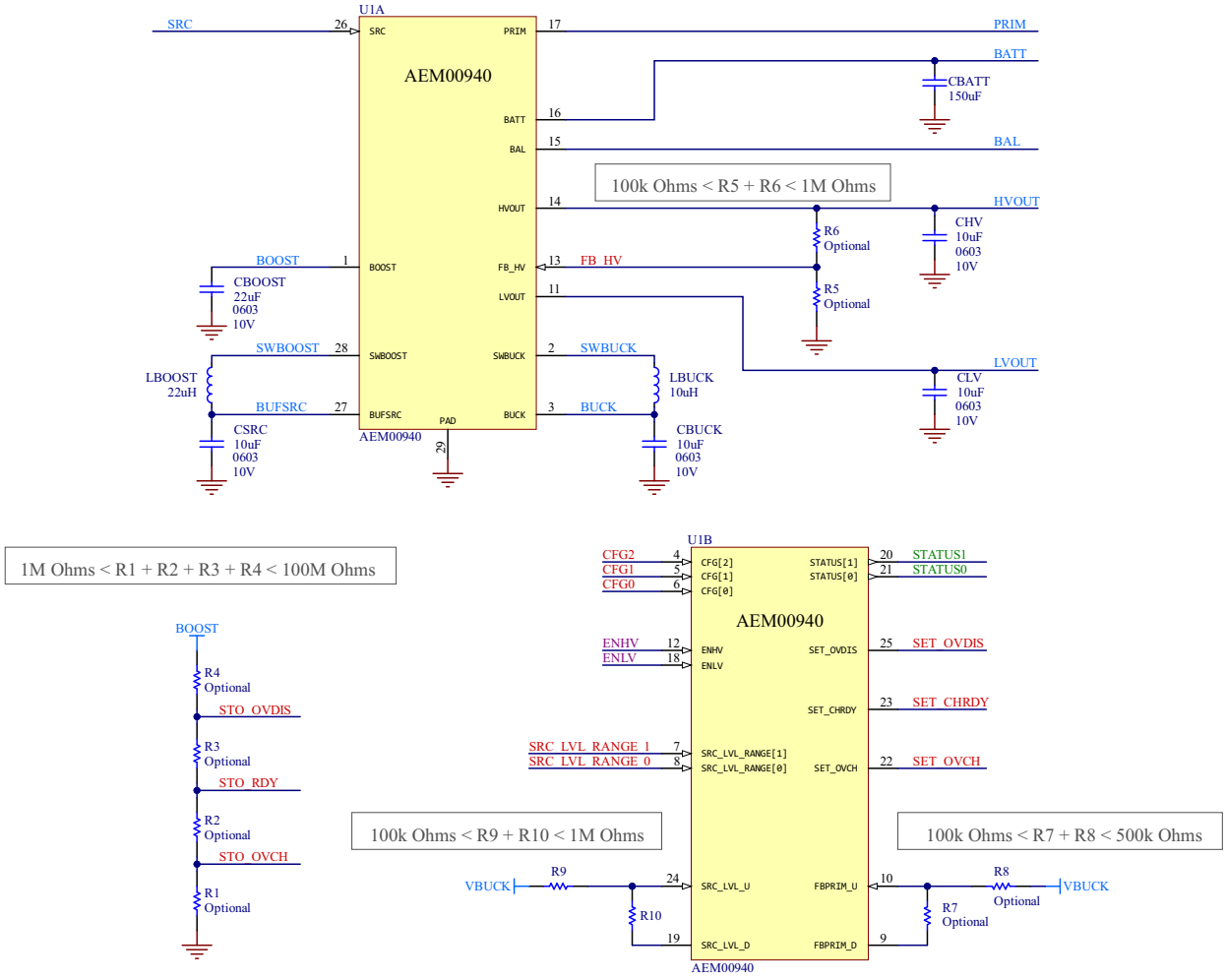
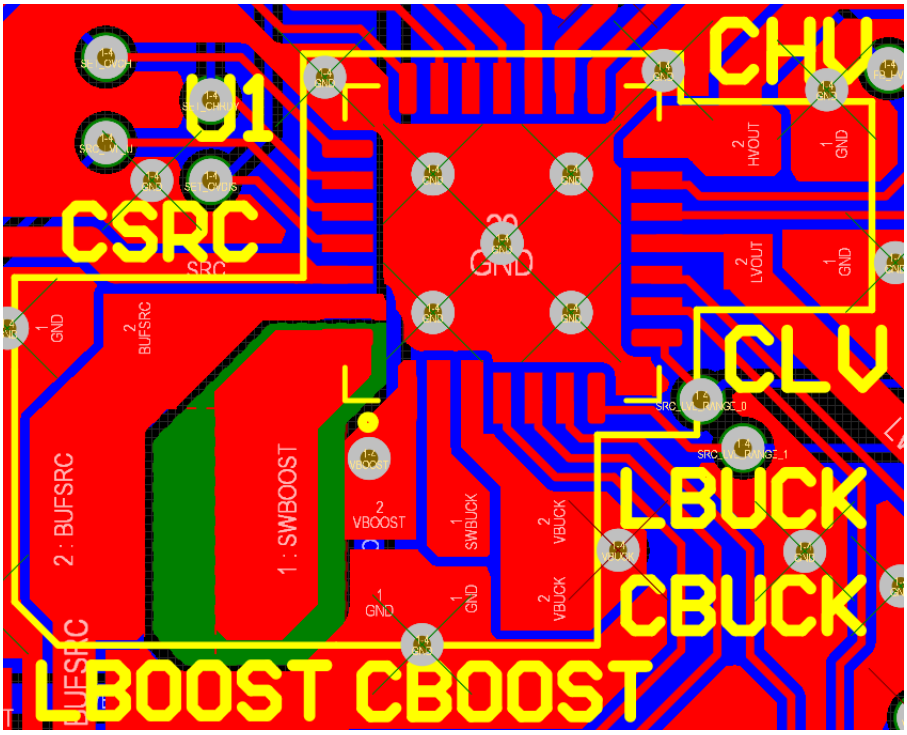


Figure 19: Schematic example

12. Layout



13. *Layout example for the AEM00940 and its passive components*Package Information

13.1. Plastic Quad Flatpack No-lead (QFN 28-pin 5x5mm)

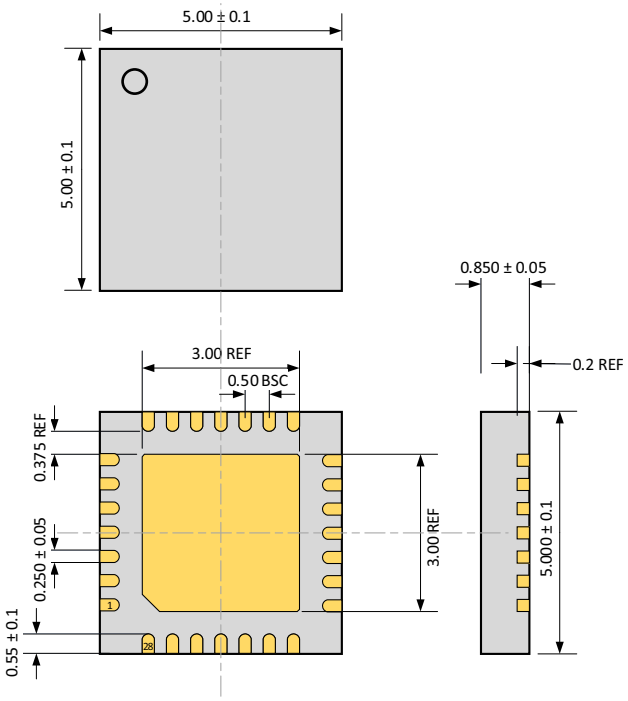


Figure 20: QFN 28-pin5x5mm drawing (all dimension in mm)

13.2. Board Layout

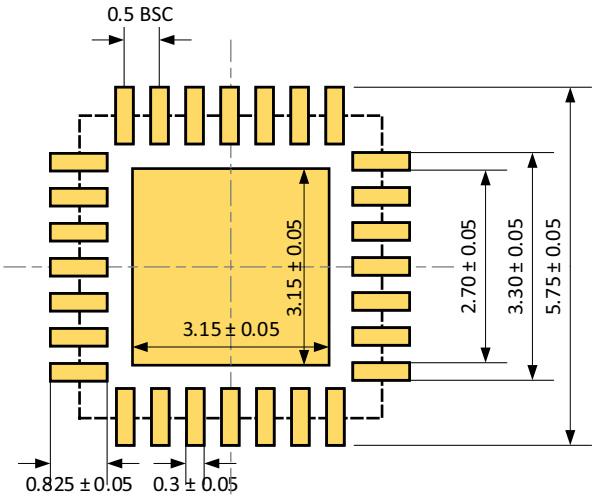


Figure 21: Recommended board layout (all dimension in mm)

14. Revision History

Revision	Date	Description
1.0	February, 2022	Creation of the document

Table 11: Revision history