




SIG100 – UART/LIN over Powerline Transceiver

1. Overview

The SIG100 is a byte-oriented UART/LIN transceiver over DC powerline (DC-BUS). The device merges both data and power over the powerline, eliminating the need for control and data wires. The SIG100 is an advanced generation of the widely used SIG60 device. Both devices use a unique multiplex digital signaling technology that overcomes the powerline noisy environment at bitrates up to 115.2Kbit/s. Sleep mode allows low power consumption when the device is not used. A small size QFN32 5x5 mm package delivers small PCB footprint .

The SIG100 powerline transceiver is useful for a wide range of automotive, aerospace and industrial applications. These include networks for sensor readings, actuator activation, battery monitoring (BMS), doors, seats, mirrors, climate control, lights, Truck-Trailer communication, etc.

The SIG100 can remotely access over the powerline up to 255 x SIG102 devices and control their eight I/O pins. Each I/O pin can be configured as either built-in A/D input or digital input or digital output or PWM output. It is mainly useful in sensors actuators networks and variety of other remote control applications.

Applications

- Vehicle sub-bus(es)
- Battery management (BMS)
- Climate control network
- Sensors / actuators bus
- Robotics control networks
- Lighting control
- Truck-Trailer communication
- Multiple networks sharing the same powerline

Features

- Noise robust UART/LIN transceiver over DC powerline.
- Selectable bitrates from 9.6kbit/s up to 115.2kbit/s
- 251 selectable carrier frequencies (5MHz to 30MHz) for multiple networks over single powerline.
- No limit to the number of bytes in a message.
- Operates as Master or as a Slave in a multiplex network.
- Communicates over wide range of DC voltages.
- Eliminates data wire and transceiver in LIN bus
- Power management (Sleep modes) for low power consumption.

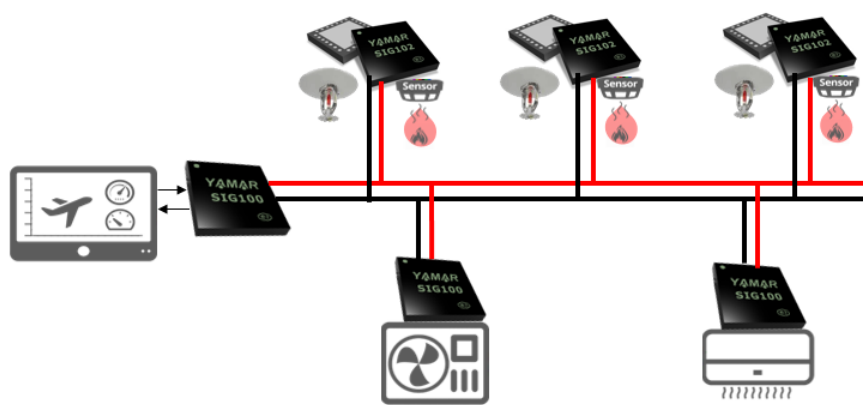


Figure 1- SIG100 /SIG102 combined climate control and fire sensing powerline network

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2. Description

2.1 The SIG100 in a network

The SIG100 transfers over powerline half-duplex peer-to-peer communication or operates as Master-Slaves network of multiple SIG100 and optional SIG102 devices. User can define its own protocol since there is no limit to the number of UART bytes in a message. Furthermore, the SIG100 operates on any selectable carrier frequency between 5MHz and 30MHz with 100 kHz spacing, so multiple independent networks may operate over the same powerline using a different carrier frequency for each network. It is recommended to keep at least 1MHz spacing between two carriers (networks).

Two alternate user-pre-defined frequencies allow hopping between these frequencies using *FREQ_SEL[1:0]* pins. This feature is useful when communication fails on the main frequency (see section 3.4.2 - Carrier frequency management).

Figure 2 depicts a typical SIG100 network, demonstrating a single byte transmission from SIG100 TX device to three SIG100 RX devices coupled through $C_{coupling}$ to the same powerline. Upon detection a start bit on the Tx SIG100 TX device HDI pin, a powerline *PLC-byte* transmission begins. After latency of ~ 2.5 bits, the powerline *PLC-byte* is decoded back to a *byte-field* on SIG100 RX devices' HDO pin.

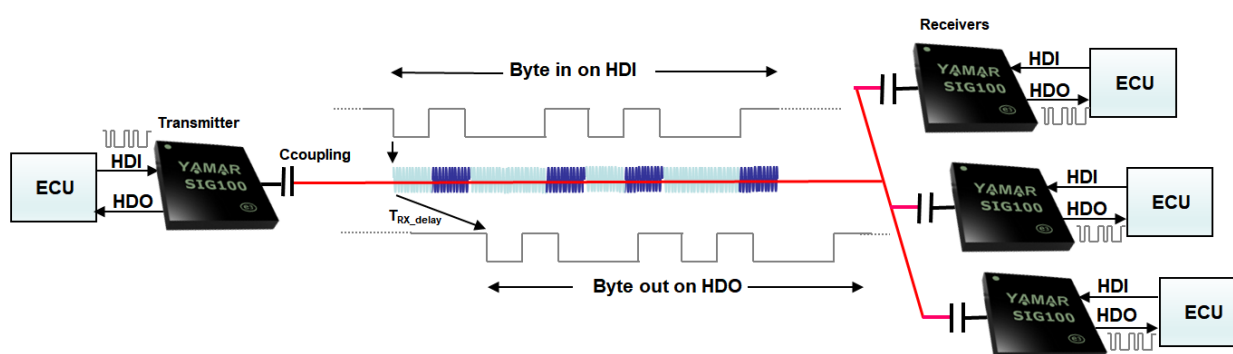


Figure 2 – SIG100 byte oriented network

2.1.1 SIG100 channel parameters

Carrier frequency:	251 selectable frequencies between 5MHz - 30MHz with 100 kHz spacing.
Powerline bitrate:	9.6kbit/s, 10.4kbit/s, 19.2Kbit/s, 38.4Kbit/s, 57.6kbit/s, and 115.2kbit/s.
Powerline voltage:	Any, with proper powerline coupling interfacing (see 2.5.8)
Cable length:	Depends on the powerline AC loads signal attenuation (100m is practical)
Cable type:	Any cable.

2.2 The Signaling technology

The SIG100 uses for its operation a unique Signaling technology. Each UART *byte-field* transferred to the device constructs a multiphase signaling *PLC-byte* carrier over the powerline that is decoded in the receiving device back into a UART *byte-field*. There is no restriction to the number of bytes transferred. The device supports also a *break-field* such as in LIN protocol by generating *PLC-Break* over the powerline that is translated back by all receiving devices back into *Break-field*. It allows seamless interfacing with existing LIN network to be conveyed LIN over the powerline.

2.3 SIG100 architecture

Figure 3 depicts the SIG100 building blocks.

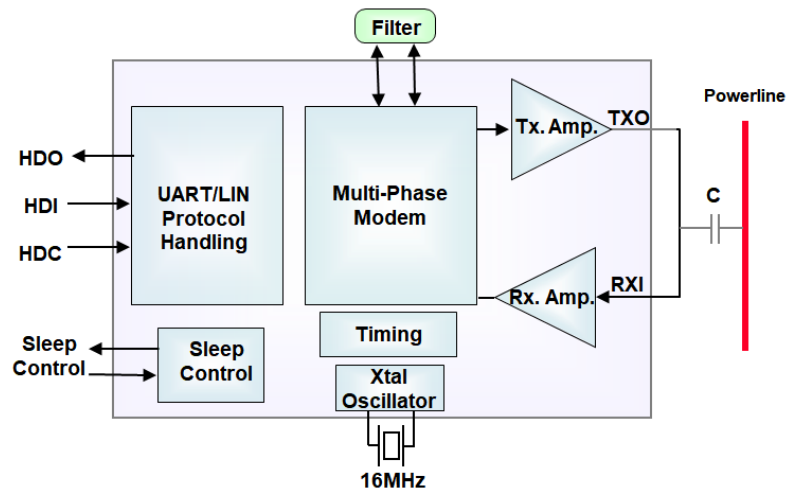


Figure 3- SIG100 Logical Blocks

The SIG100 main building blocks:

- **Protocol handler** - Interface with UART/LIN ECU.
- **Multi-Phase Modem** - Phase modulates and demodulates the UART bytes to/from the DC-BUS powerline.
- **Sleep control** - handles low power consumption during Sleep mode.

2.4 Pin configuration and function

2.4.1 Pin diagram

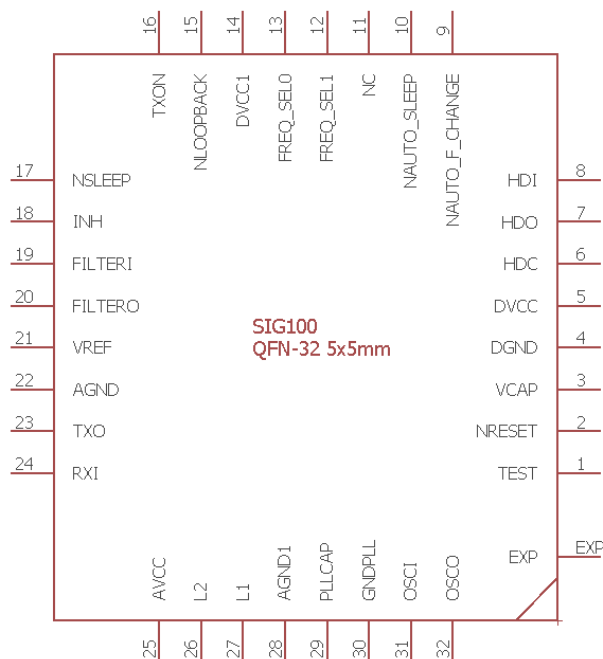


Figure 4 – SIG100 pinout diagram in QFN32 5x5mm package

2.4.2 Signals and Pinout description

Table 1 - Pinout description

Name	Pin #	Pin type	Internal PU/PD	Description																		
HDO	7	Output 12mA		Outputs the received data from the powerline or from internal registers to the ECU.																		
HDI	8	Digital input	PU	Transfers data from the ECU to the powerline or to the internal registers.																		
HDC	6	Digital input	PU	ECU Data / Command input. When low, enables read and write from/to the SIG100 control registers (see section 5.14 0).																		
TEST	1	Digital Input	PD	Should be connected to Gnd.																		
NRESET	2	Digital Input	PU	Reset, active low.																		
NSLEEP	17	Digital Input		Sleep mode control input (see section 4.3). Should be pull-up to 3.3V when not in use.																		
NAUTO_F_CHANGE	9	Digital Input		When low, the SIG100 will automatically hop between main carrier frequency and two alternate frequencies (see 3.4.4).																		
NAUTO_SLEEP	10	Digital Input		When low, the SIG100 automatically enters Sleep mode when there is no transmission or reception to/from the powerline longer than <i>AutoSleep-timeout</i> setting (see 4.4).																		
NC	11			Should be left floated.																		
NLOOPBACK	15	Digital Input	PU	When high, loopback from HDO to HDI is disabled (see 3.4.5)																		
INH	18	Output 8mA		When high, SIG100 is in Normal mode When low, SIG100 is in Sleep mode																		
FREQ_SELO	13	Digital Input		Main and 2 alternate frequencies selection control (see 3.4.2)																		
FREQ_SEL1	12	Digital Input		<table><tr><th>FREQ_SEL[1:0]</th><th>Default Frequency [MHz]</th><th></th></tr><tr><td>'00','11'</td><td>13</td><td>Main</td></tr><tr><td>'01'</td><td>5</td><td>Alternate 1</td></tr><tr><td>'10'</td><td>22</td><td>Alternate 2</td></tr></table>	FREQ_SEL[1:0]	Default Frequency [MHz]		'00','11'	13	Main	'01'	5	Alternate 1	'10'	22	Alternate 2						
FREQ_SEL[1:0]	Default Frequency [MHz]																					
'00','11'	13	Main																				
'01'	5	Alternate 1																				
'10'	22	Alternate 2																				
TXON	16	Output 12mA		TX_ON output - High during transmission over the powerline.																		
TXO	23	Analog Output Max 66 mA		<table><tr><th colspan="4">Powerline Transmit signal out</th></tr><tr><th>TXON State</th><th>REG_1[4]</th><th>TX level [V-p-p]</th><th>Impedance [Ω]</th></tr><tr><td rowspan="2">High</td><td>'0'</td><td>1</td><td rowspan="2">18¹</td></tr><tr><td>'1' (Default)</td><td>2</td></tr><tr><td>Low</td><td></td><td>High Z</td><td>200k²</td></tr></table> ¹ Series output impedance ² Input impedance referenced to VREF	Powerline Transmit signal out				TXON State	REG_1[4]	TX level [V-p-p]	Impedance [Ω]	High	'0'	1	18 ¹	'1' (Default)	2	Low		High Z	200k ²
Powerline Transmit signal out																						
TXON State	REG_1[4]	TX level [V-p-p]	Impedance [Ω]																			
High	'0'	1	18 ¹																			
	'1' (Default)	2																				
Low		High Z	200k ²																			
RXI	24	Analog Input		Powerline receive Input																		
VREF	21	Analog Output		VCC/2 Analog voltage reference output to a filtering capacitor. Place 1uF between VREF to AGND. VREF is a virtual ground for the external analog circuitry.																		
FILTERI	19	Analog, Bi-directional		External filter I/O																		
FILTERO	20	Analog, Bi-directional		External filter I/O																		
OSCO	32	Analog output		16MHz Crystal Output																		
OSCI	31	Analog Input		16MHz Crystal Input																		
L1	27	Analog Input		External inductor L1 (keep short trace connection), see 2.5.4.																		
L2	26	Analog Input		External inductors L2 (optional), see 2.5.4.																		
AVCC	25	Power		Analog 3.3V supply																		
AGND	22,28	Power		Analog ground																		
VCAP	3	Power		1.8V core supply output to a filtering capacitor. Place 4.7uF between VCAP and DGND.																		
DGND	4	Power		Digital Ground																		

Name	Pin #	Pin type	Internal PU/PD	Description
DVCC	5,14	Power		Digital 3.3V supply
GNDPLL	30	Power		Analog Ground
PLLCAP	29	Power		PLL 1.8V output to a filtering capacitor. Place 1uF between PLLCAP and GNDPLL.
EXP	33	Power		Expose pad, should be connected to DGND.

PD – Internal Pull down resistor 50K Ω +/-%30

PU – Internal Pull up resistor 50K Ω +/-%30

2.5 Implementation

2.5.1 SIG100 recommended schematic

Figure 5 depicts a typical SIG100 schematic.

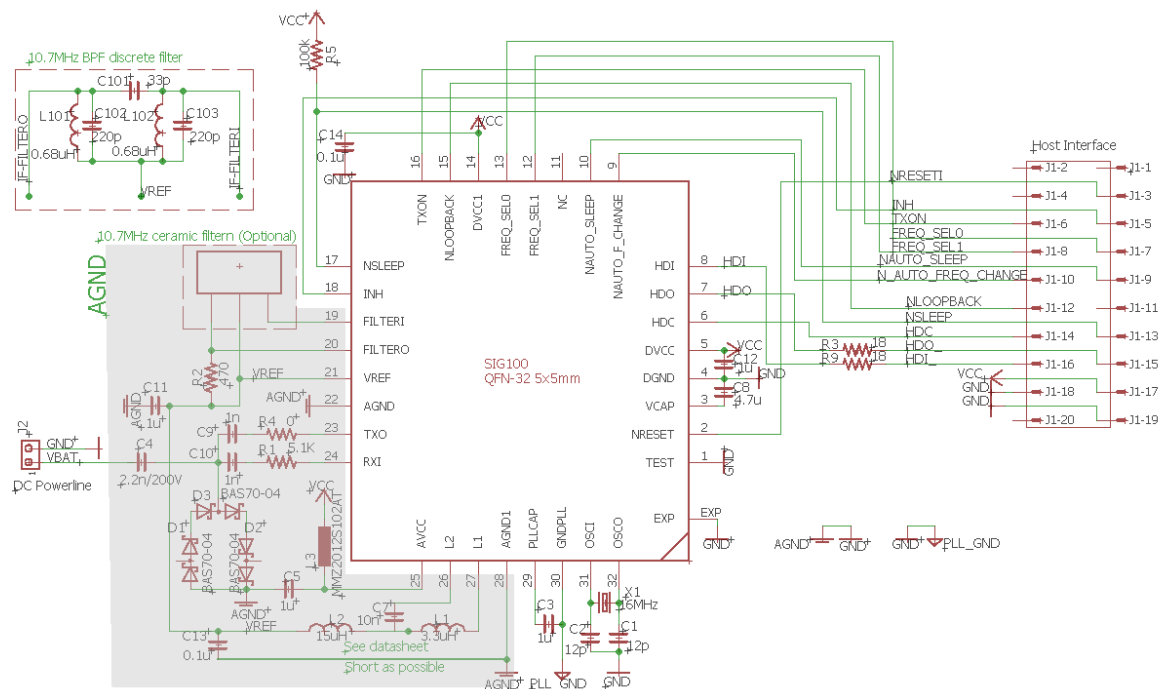


Figure 5 – SIG100 reference schematic

2.5.2 External 10.7MHz filter (BPF)

The SIG100 operates using an external 10.7MHz narrow band pass filter. The minimum recommended filter bandwidth is 330 kHz @ 3dB. Narrower bandwidth limits the maximal SIG100 bitrate.

Figure 6 depicts recommended 10.7MHz discrete filter.

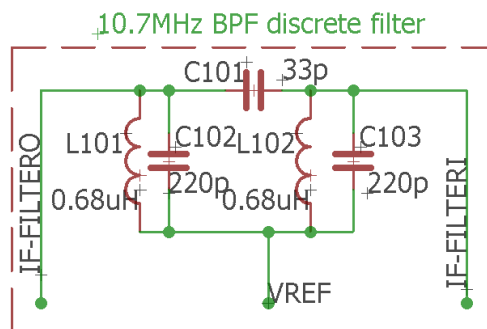





Figure 6 - 10.7MHz discrete bandpass filter

Alternatively, Table 2 describes recommended 10.7MHz ceramic filters.

Table 2 – Recommended 10.7MHz ceramic filters

Manufacturer	Part #	3dB BW [kHz] min.	Insertion loss [dB] max.	Stop band attenuation [kHz]	In/Out impd. [Ω]	Package
Murata	SFECF10M7EA00-R0	330	3.0	700	330	 SMD
Oscilent	762-0107-A20	330	3.0	700	330	 SMD
AEC	LTCV10.7MA19	350	3.0	950	470	 SMD

2.5.3 Crystal oscillator

The device operates with a low cost, small size 16MHz crystal connected between OSCI and OSCO pins. Each of these pins should be connected to the DGND via a load capacitor. The load capacitors values should be determined according to the crystal manufacturer recommendations and the actual PCB layout. The PCB traces should be as short as possible.

The overall frequency tolerance should not exceed $\pm 50\text{ppm}$.

- Recommended crystals:**

- NDK NX2520SA-16MHz SMD, 2.5x2 mm
- NDK NX3225SA/GB-16MHz SMD, 3.2x2.5mm
- NDK NX2016GC-16MHz SMD, 2.0x1.6mm

2.5.3.1 16MHz clock from external source

The device can operate from external 16MHz clock that meets the requirements above.

Figure 7 depicts external 16MHz clock connection to the device.

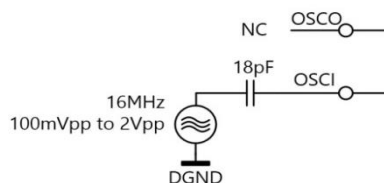


Figure 7 - External 16MHz clock connection

2.5.4 L1 and L2 inductors

The SIG100 requires one or two inductors for its operation, depending on the desired operating frequency.

- For full in-band operation, 5MHz - 30MHz:

- L1 - 3.3uH
- L2 - 15uH with 1nF series capacitor between L2 pin and L2 inductor.

- For low in-band operation, 5MHz -12MHz:

- L1 - 18uH
- L2 - NC

- For high in-band operation, 12MHz - 30MHz:

- L1 - 3.3uH
- L2 - NC

Figure 8 depicts in-band operation inductors connection to pins L1 and L2.

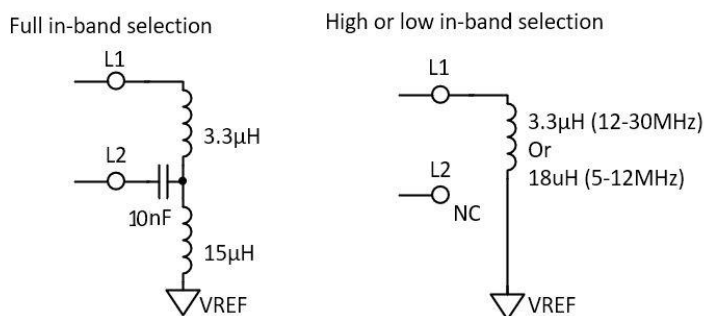


Figure 8 - L1 and L2 inductors connections

2.5.5 Recommended L1 & L2 inductors

Table 3 describes recommended L1 and L2 inductors.

Table 3 - Recommended L1 and L2 manufacturers

Inductor	ABRACON	VISHAY	TDK
L1=3.3uH	815-AIML-0805-3R3K-T	ILSB0805ER3R3K	NL453232T-3R3J-PF
L2=15uH	815-AIML-0805-150K-T	ILSB0805ER150K	NL453232T-150J-PF
L1=18uH	815-AIML-0805-180K-T	ILSB0805ER180K	NL453232T-180J-PF

2.5.6 Ceramic capacitors

Low ESR capacitors will provide better performance. X5R and X7R capacitors are recommended, especially for Vcap (C8) and PLLCAP (C3).

2.5.7 TXO output level and drive control

The TXO pin output level and drive capability to the powerline is controlled by REG_1[4], as described in Table 4.

Table 4 - TXO signal level

TXON State	REG_1[4]	TX level [V-p-p]
High	'0'	1
	'1' (Default)	2
Low (Rx)		High Z

Set the TXO output drive capability by configuring REG_1[7], as described in Table 5.

Table 5- TXO output drive control

TXON State	REG_1[7]	Output drive [A]	Impedance [Ω]
High	'0' (Default)	33mA	18 ¹
	'1'	66mA	
Low (Rx)		Disabled	200k ²

¹Series output impedance

²Input impedance referenced to VREF

2.5.8 Powerline coupling interface

The SIG100 is coupled to the powerline through a single small footprint DC blocking ceramic capacitor, typically 2.2nF. The C_{coupling} voltage rating depends on the powerline voltage and its expected impulses. For high voltage powerline applications (e.g. battery monitoring system in EV or solar panels), it is required to add galvanic isolation.

2.5.9 External protection network

Simple external diode protection network is recommended prior to the C_{coupling}, to protect against high powerline pulses (above 2 V-P-P). The protection network consists of three low capacitance (< 10pF) fast schottky diodes serially connected in both polarities (e.g. BAS70-04).

2.5.10 Recommended connection to power-supply

Power-supplies have filtering capacitors in its DC inputs. These capacitors attenuate strongly the SIG100 carrier signal. It is recommended to add an inductor ($>22\mu\text{H}$) or ferrite bead ($>100\Omega$ @ 5MHz-30MHz) in series to the power-supply connection to the DC powerline to reduce the carrier signal attenuation.

Figure 9 depicts a typical SIG100 connection to a DC powerline and to its 3.3V power-supply.

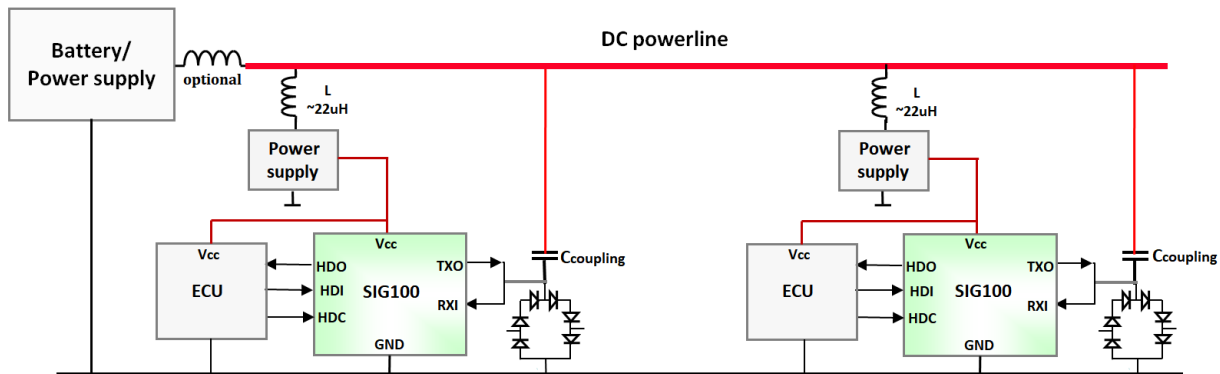


Figure 9 – SIG100 connection to 3.3V power-supply and powerline

3. Operation

3.1 Interfacing to UART/LIN ECU

The SIG100 interfaces directly to any uC UART/LIN I/O pins (3.3V logic).

The UART/LIN communication protocol uses four pins as described in Table 6.

Table 6 – UART/LIN interface pins

SIG100	ECU	Description
HDI	Tx	Data Input from the host ECU.
HDC	GPO	Data/Command select input. When pulled down, the SIG100 enters command mode, enabling access to SIG100 internal registers.
HDO	Rx	Data output to the host ECU.
NLOOPBACK	GPO	Enable loopback of HDI to HDO pin. When interfacing a UART port, ECU may disable/enable the loopback option. When interfacing a LIN transceiver, loopback disabled by keeping pin floated (internal PU). When interfacing a LIN ECU, tie pin to GND. HDI loops back to HDO.

Figure 10 depicts a typical SIG100 to ECU UART/LIN interface connection.

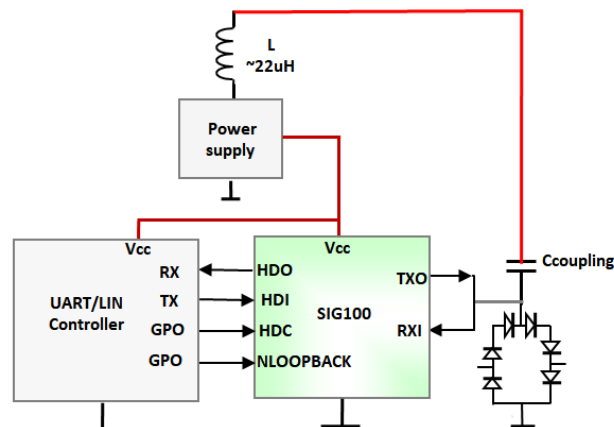


Figure 10 - Typical SIG100 to UART/LIN ECU interface

3.2 Interfacing to existing LIN module

When interfacing to a LIN module that has already built-in LIN transceiver, additional LIN transceiver is required to translate the signals to Tx and Rx 3.3V logic. The loopback between HDI and HDO pins has to be disabled. Keep NLOOPBACK pin floated.

Figure 11 depicts a typical SIG100 to LIN transceiver interface connection.

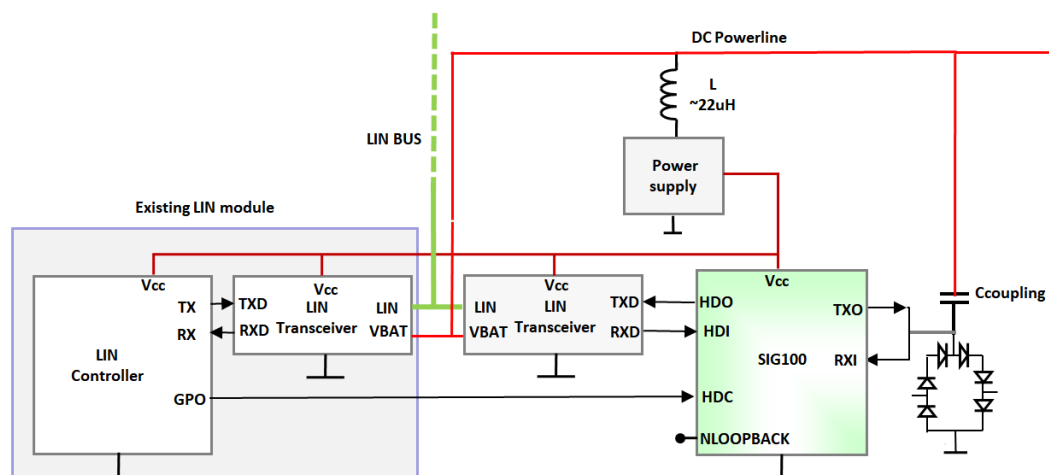


Figure 11 - Typical SIG100 to LIN transceiver interface

3.3 SIG100 messages

3.3.1 Message structure

The SIG100 supports UART and LIN protocols.

- A *byte-field (UART byte)* is defined with one start bit, 8 data bits, and one stop bit.
- A *PLC-byte* is defined as the signaling pattern of the *byte-field* over the powerline.
- A *break-field* is defined as one start bit, 12 to 30 zero bits, and one stop bit.
- A *PLC-break* is defined as the signaling pattern of the *break-field* over the powerline

The SIG100 is a byte-oriented powerline transceiver. Each UART/LIN *byte-field* on HDI pin is encoded into a modulated powerline *PLC-byte* at the length of the ECU UART bitrate. At the receiving side, each *PLC-byte* is decoded back after fixed delay of $\sim 2.5T_{bit}$ to HDO *byte-field*. A *break-field* at the beginning of a LIN message is handled the same.

3.3.2 Transmit flow

Upon detection of a start bit on HDI, the SIG100 starts its *byte-field/break-field* transmission over the powerline until receiving a stop bit from ECU. In case ECU transfer bytes continuously (i.e. inter-byte spacing between bytes $< 1/3 T_{bit}$), the SIG100 will not stop its transmission. If the inter-byte space is longer than $1/3 T_{bit}$, the SIG100 will stop its transmission over the powerline and will wait for the next start bit.

3.3.3 Receive flow

Upon detection of a powerline *PLC-byte/PLC-break*, the SIG100 will decode the *PLC-byte* and transfer the *byte-field* to the receiving ECU's HDO pin (a start bit followed by the data bits and stop bit).

The delay (powerline latency) between Transmitter start bit drop on HDI to Receiver start bit drop is $T_{RX_delay} = \sim 2.5 T_{bit}$.

Figure 12 depicts a single *byte-field* \rightarrow *PLC-byte* \rightarrow *byte-field* TX-RX flow. ECU A transfers 0x55 *byte-field* on HDI with local loopback feedback on HDO (loopback is enabled). Upon start bit detection, a powerline transmission of *PLC-byte* 0x55 (length of $10 \times T_{bit}$), begins. Then, after T_{RX_delay} of $\sim 2.5 T_{bit}$, the *PLC-byte* is extracted on RX device B HDO pin to its ECU.

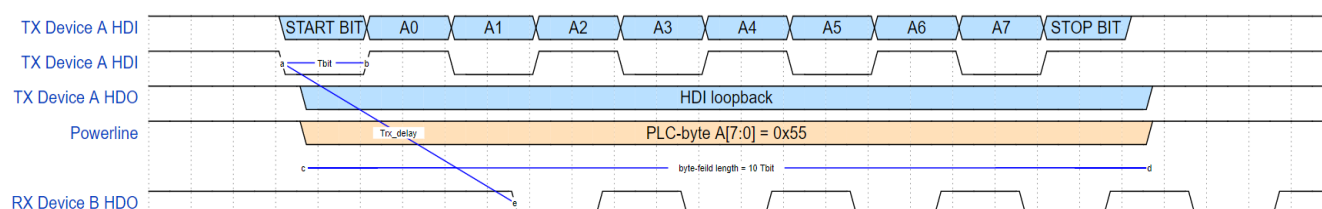


Figure 12 – SIG100 single *PLC-byte* TX-RX example

Figure 13 depicts a single *break-field* TX-RX flow. ECU A transfers a *break-field* on HDI with local loopback feedback on HDO (loopback is enabled). Upon start bit detection, a powerline transmission of *PLC-break* (length of $13 \times T_{bit}$), begins. Then, after T_{RX_delay} of $\sim 2.5 T_{bit}$, the *break-field* is extracted on RX device B HDO to its ECU.

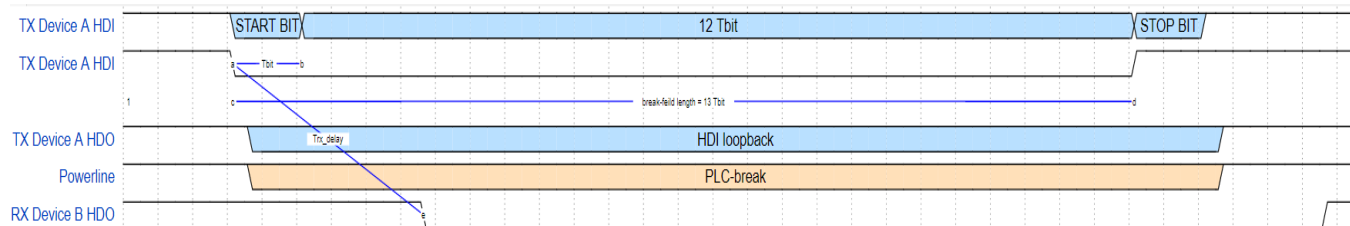


Figure 13 – SIG100 single *break-field* TX-RX example

3.4 Device configuration

3.4.1 Bitrate configuration

Table 7 describes the SIG100 supported bitrate selection.

Bitrate configuration is made by setting REG_0[2:0] bits using *WRITE-REG* command (see 5.14.1).

Table 7 – Bitrate selection

REG_0 Bitrate_sel[2:0]	Bitrate [bit/s]	T_{bit} [μs]
000	9600	104
001	10417	96
010	19200 (default)	52
011	38400	26
100	57600	17.36
101	115200	8.68

3.4.2 Carrier frequency management

The SIG100 operates on its configured main frequency. Two alternate frequencies (ALT1 and ALT2) are available for frequency hopping in case that the operating frequency is blocked by interference.

The active working frequency is determined by *FREQ_SEL*[1:0] hardware pins setting. For each change in *FREQ_SEL*[1:0] pins, the SIG100 will switch to the selected carrier frequency (Main/ALT1/ALT2) according to Table 8 mapping.

Set the Main/ALT1/ALT2 frequencies by configuring REG_2/ REG_3/ REG_4 respectively (see 5.14.1).

For each configuration of REG_2, the active frequency is automatically switched to the Main frequency (as set in REG_2), regardless of *FREQ_SEL*[1:0] pins setting. Switching to ALT1/ALT2 again, will take place only at the next change of *FREQ_SEL*[1:0] pins.

ECU may read the active operating carrier frequency value stored in read-only REG_5.

Table 8 describes the carrier frequency setting and control.

Table 8 – Carrier frequency setting and control

Carrier Frequency	<i>FREQ_SEL</i> [1:0]	Register name	Default Frequency [MHz]
Main	'00','11'	REG_2[7:0]	13
ALT1	'01'	REG_3[7:0]	5
ALT2	'10'	REG_4[7:0]	22

3.4.3 Carrier frequency configuration

ECU can define carrier frequency from 5MHz to 30MHz with spacing of 100 kHz (Total of 251 selectable carriers). Upon completion of configuration or change of `FREQ_SEL[1:0]` pins, the SIG100 will update its operating carrier frequency within 1msec period. During this period, the SIG100 is kept in *Soft-Reset* and will not communicate with its ECU nor detect new messages from the powerline.

When multiple SIG100 networks operate over single powerline, it is recommended to select their carrier frequencies spaced more than 1MHz between each other.

The carrier-selected value is calculated the as given in Equation (3).

Equation 1

$$\text{REG_2/3/4} = (\text{Carrier Freq. [MHz]} - 5) * 10 \quad (1)$$

EXAMPLE 1

- ❖ When setting the frequency to 14.1MHz:
 $\text{REG_2/3/4} = (14.1 - 5) * 10 = \text{0x5B}$

EXAMPLE 2

- ❖ When Setting to 5MHz:
 $\text{REG_2/3/4} = (5 - 5) * 10 = \text{0x00}$

3.4.4 Auto frequency change mode

The Auto frequency change mode is enabled either by pull `NAUTO_F_CHANGE` pin low or by clearing `REG_0[3]` bit. Last action prevails.

When enabled, the SIG100 automatically hops between Main, ALT1, or ALT2 configured frequencies when no powerline *PLC-byte* activity detected more than 2 sec. It indicates that neither transmission nor reception detected over the powerline.

The hopping method is as follows:

Main ---> ALT1 ---> Main ---> ALT2 ---> Main ...

3.4.5 Loopback

LOOPBACK between HDI and HDO is required when interfacing to a LIN ECU. Loopback has to be disabled when interfacing a LIN transceiver (see 3.1).

Loopback is enabled either by pull `LOOPBACK` pin low or by clearing `REG_0[5]`. Last action prevails.

3.4.6 Remote loopback mode

The remote loopback function, when enabled, triggers the SIG100 transmits-back its last received powerline *PLC-byte* over the powerline. This function is useful in point to point communication between two SIG100/SIG102 devices as part of ECU built-in ACK/NACK mechanism. For example, the checksum byte at the end of a message is returned to the transmitting Master to validate the integrity of the received message by the Slave.

Remote loopback mode is enabled by setting `REG_0[4]`. The SIG100 RX device will response back only when the powerline is idle for at least $3 \times T_{\text{bit}}$ time after full reception of last byte.

Figure 14 depicts an example of remote loopback operation. ECU A transfers two data bytes [0x00][0x01] that are transmitted over the powerline to ECU B. Upon detecting the last transmitted 0x01 byte, SIG100 device B waits for $3 \times T_{\text{bit}}$ time before automatically transmit-back 0x01 over the powerline to device A.

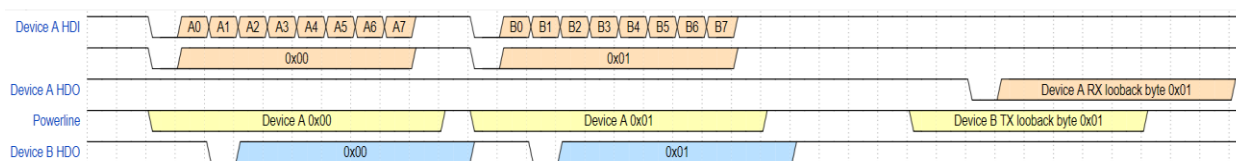


Figure 14 – Remote loopback example

3.4.7 SIG100 UUID

Each SIG100 device is hard-coded with 48 bit universally unique identifier (UUID[47:0]).

The UUID is stored in REG_96 to REG_9B, and can be retrieved using the READ-REG commands (see 5.8 to 5.13).

3.4.8 Typical set-up and operation example

1. Interface HDI, HDO, and HDC pins to the host ECU.
2. Enable/disable loopback of HDI pin to HDO pin (see 3.4.5).
3. Select SIG100 bitrate according to ECU UART/LIN bitrate (see 3.4).
4. Select a carrier frequency (default 13MHz) (see 3.4.2).
5. Transmit bytes via HDI pin to the powerline.
6. Receive bytes from the powerline via HDO pin.

4. Power Operation Modes

The SIG100 has three power operation modes; Normal (RX/TX), Standby and Sleep.

4.1 Normal mode

In Normal mode, the SIG100 is either in RX mode, listening for a powerline *PLC-byte* and *PLC-break*, or in TX mode, transmitting a message over the powerline.

4.2 Standby mode

The SIG100 enters Standby mode upon wake-up from Sleep mode, while NSLEEP pin is still low. The SIG100 is kept in *Soft-Reset*, whereas communication with the ECU is suspended until NSLEEP pin set High.

4.3 Sleep modes (power-saving)

The SIG100 has four Sleep modes for best power consumption/performance during Sleep. During this mode, only small amount of hardware operates to detect wake-up messages (*WUM*) from the powerline and return to Normal mode operation.

Four interface pins are used for Sleep modes operation, as described in Table 9.

Table 9- Sleep interface pins

NSLEEP	Digital input	High - Normal mode is active. Low - Sleep /Standby mode is active. Upon transition from low to high, WUM is transmitted over the powerline.
INH	Digital output	Output indication to Inhibit the ECU. High - Normal mode is active. Low - Sleep mode is active.
HDO	Digital output	Normal mode - data output to ECU. Sleep/Standby mode - asserted low while wake-up message (WUM) is being detected/transmitted over the powerline.
HDC	Digital input	Normal mode – ECU's Host Command mode. Sleep mode - ECU wakes-up the SIG100 locally by toggling the HDC high-low-high. The SIG100 then exit the Sleep mode to Standby mode (NSLEEP still asserted low), or Normal mode (NSLEEP is high).

4.3.1 Wake-up message (WUM)

When *Auto-WUM* is enabled (*REG_6[6]='1'*), upon rise of NSLEEP pin the SIG100 transmits a *WUM* over the powerline to wake-up all network connected devices.

ECU can configure the length of the WUM as described Table 10.

Table 10 - Wake-up message length configuration

<i>REG_6[4]</i>	Wake-up message length
0	<i>SLP2</i> - 250usec / <i>SLP1, SLP3</i> - 75msec
1	<i>SLP2</i> - 1.5msec / <i>SLP1, SLP3</i> - 150msec

During WUM transmission, the HDO pin is asserted low until WUM transmission is completed, indicating to the ECU the wake-up process status. ECU shall wait for the HDO rise before initiating new bytes transfer.

4.3.2 Entering Sleep mode

During Sleep mode, the device is kept in *Soft-Reset* state and will not transfer bytes from the ECU nor receive bytes from the powerline. When the device enters Sleep mode, the INH pin is asserted low.
There are two ways to enter Sleep mode;

4.3.2.1 Enter Sleep by NSLEEP pin

By asserting the NSLEEP pin low, the SIG100 will enter Sleep mode.

4.3.2.2 Enter Sleep by register setting

By setting *REG_6[7]* high, the SIG100 will enter Sleep mode, and reset automatically *REG_6[7]* to low.

4.3.3 Exiting Sleep mode

There are three ways to exit Sleep mode. When exiting Sleep mode, the INH pin is raised and the device switches to Standby or Normal mode.

4.3.3.1 Exit Sleep by WUM detection

Upon detection of a *WUM*, the device exits Sleep mode, INH pin raises and device enters Standby mode.
In case NSLEEP pin is low, the device remains in Standby mode, where the device is kept in *Soft-Reset*.
In case NSLEEP pin is high, the device switches to Normal mode.

During WUM reception, the HDO pin is asserted low until WUM reception is completed, indicating the ECU on the wake-up process status. ECU shall wait for HDO to rise, before initiating new bytes transfer.

4.3.3.2 Exit sleep by NSLEEP pin

Upon detection of NSLEEP pin rise, the device exits Sleep mode, INH pin rises, and enters Normal mode. When *Auto-WUM* enabled, a WUM is transmitted over the powerline (see 4.3.1).

4.3.3.3 Exit Sleep by HDC toggling

Upon detection of HDC pin toggle high-low-high, the device exits Sleep mode, INH pin rises and enters Standby mode.
In case NSLEEP pin is still low, the device remains in Standby mode, where the device is kept in *Soft-Reset*.
In case NSLEEP pin is high, the device switches to Normal mode.
In this case, the **WUM is NOT transmitted** over the powerline.
ECU shall use the HDC pin to exit Sleep mode, when the NSLEEP pin is not connected.

4.3.4 Sleep modes description

ECU can select between four Sleep modes (see 5.7). Table 11 describes the SIG100 sleep modes.

Table 11 - Sleep modes description

Sleep mode	Description	Power consumption	Performance
Enhanced sleep (SLP1)	The device wakes-up every 32ms to sense the powerline for WUM detection.	Low	Wake-up detection with-in 64mSec. Best detection in noisy environment.
Fast wake-up (SLP2)	The device continuously monitors the powerline for WUM detection.	Medium	Fast wake-up detection with-in 250uSec.
Very low-power (SLP3)	The device wakes-up every 32ms to sense the powerline for WUM detection.	Very low	Wake-up Detection with-in 64mSec.
Deep Sleep (SLP4)	The device does NOT wake-up to sense for bus activity, staying in deep sleep. Wake-up only locally by the ECU.	Lowest	No bus wake-up detection.

4.3.4.1 Enhanced Sleep mode (SLP1)

By setting *REG_6[1:0] = '00'*, the enhanced Sleep mode (*SLP1*) is selected.
When entering *SLP1*, the device wakes-up every 32ms periodically to monitor (sense period) for activity on the powerline. If a WUM is detected, the device exits sleep mode as described in section 4.3.3.1, otherwise the device returns to Sleep mode until next sense period, and so on...

4.3.4.2 Fast wake-up Sleep mode (SLP2)

By setting $REG_6[1:0] = '01'$, the Fast wake-up Sleep mode (SLP2) is selected. The device continuously monitors the powerline for WUM detection. The WUM detection is within 250usec. When WUM is detected, the device exits Sleep mode as described in section 4.3.3.1.

4.3.4.3 Very low-power Sleep mode (SLP3)

By setting $REG_6[1:0] = '10'$, the Very low-power mode (SLP3) is selected. The device wakes-up every 32msec to sense for activity on the powerline. If a WUM is detected, the device exits Sleep mode as described in section 4.3.3.1, otherwise the device return to Sleep until next sense period, and so on.

4.3.4.4 Deep Sleep mode (SLP4)

By setting $REG_6[1:0] = '11'$, the Deep Sleep mode (SLP4) is selected. The device does NOT wake-up to sense the powerline for activity, rather than stay in deep sleep, whereas most of its hardware is shut down to maintain the lowest power consumption.

The device exits Deep Sleep mode only locally, either by NSLEEP or HDC pins (see 4.3.3.2 and 4.3.3.3).

4.4 Auto Sleep mode

Auto sleep mode is enabled either by pulling NAUTO_SLEEP pin low or by clearing $REG_6[5]$. Last action prevails.

When enabled, the SIG100 automatically enters into Sleep mode when no Transmission or reception to/from the powerline (DC-BUS idle) for more than *AutoSleep-timeout* setting.

The SIG100 exits sleep mode in case of NSLEEP/HDC pin toggling, or by WUM detection (see 4.3.3).

Table 12 describes the *AutoSleep-timeout* configuration options.

Table 12 - *AutoSleep-timeout* configuration

$REG_6[3:2]$	AutoSleep-timeout [Seconds]
00	Auto Sleep mode disabled
01	2
10	4
11	6 (default)

4.5 Sleep modes Examples

4.5.1.1 Sleep Example 1 - Enter by NSLEEP, Exit Sleep mode by NSLEEP & WUM

Figure 15 depicts entering sleep by NSLEEP and exit sleep by NSLEEP pin (Node A) and WUM detection (Node B).

In this example, the ECU wakes-up device Node A by raising the NSLEEP pin, causing the INH pin to raise and a WUM is transmitted over powerline (*Auto-WUM* is enabled) to wake-up Node B.

While transmitting the WUM, device Node A asserts HDO pin low. After completion of WUM transmission, the HDO pin is raised again (can be used as signal / interrupt to ECU). At Node B side, during its sensing period (e.g. SLP1), the WUM is detected, and the INH pin rises while switching to Standby mode. Node B HDO pin is asserted low for the reaming duration of WUM reception. Then, ECU Node B raises the NSLEEP pin, and the device switches to Normal mode.

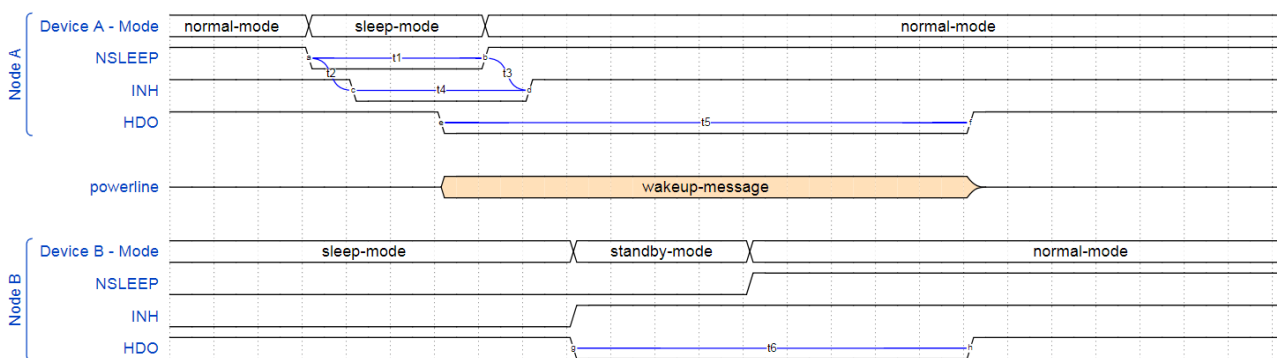


Figure 15 - Enter sleep by NSLEEP, Exit sleep by NSLEEP & WUM

4.5.1.1 Sleep Example 2 - Enter sleep by control register bit, exit sleep by HDC

Figure 16 depicts entering sleep by setting *REG_6[7]* high, and exiting Sleep mode by toggling the HDC pin. In this example, ECU configured *REG_6[7]* high using Command mode, the device enters Sleep mode and INH pin drops. After a while, ECU toggle HDC pin low to high, and the device exits Sleep mode without transmitting the WUM, raising the INH pin and switching to Normal mode again.

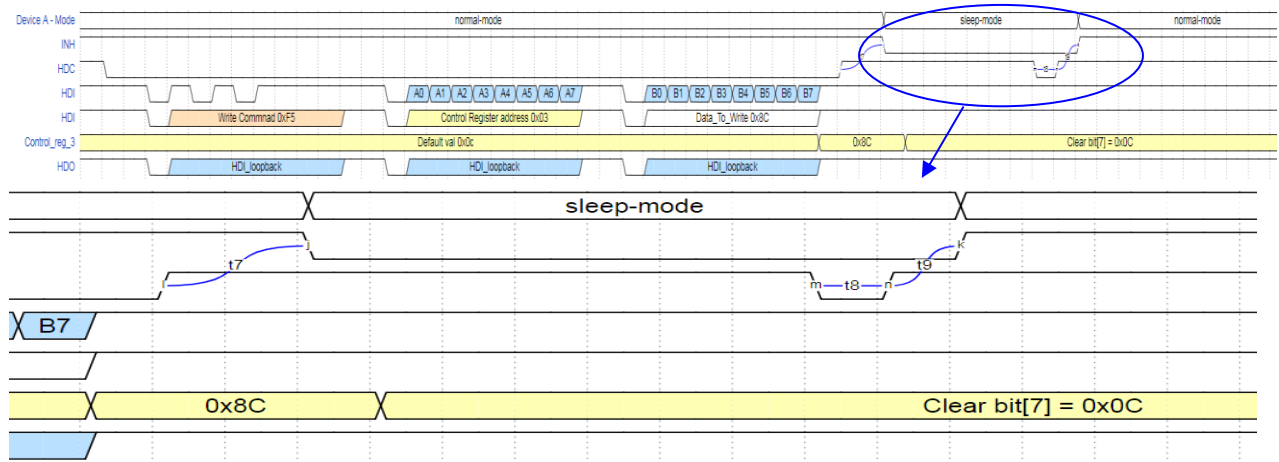


Figure 16 - Enter sleep by control register bit, Exit sleep by HDC

5. SIG100 Registers

The SIG100 internal registers are used for configuration and status check. Each register is accessible from its ECU for *Read* and *Write* operations. This section elaborates on the registers and their default values after power-up/reset. See section 0 for more details about registers configuration method.

Table 13 - Registers summary table

Register name	Addr.	Description
REG_0 - 'Device Control 0'	0x00	Bitrate selection, Loopback, nAuto_freq_change
REG_1 - 'Device Control 1'	0x01	Transmit level control
REG_2 - 'Frequency Main select'	0x02	Main Carrier frequency selection
Reg_3 - 'Frequency ALT1 select'	0x03	Alternate frequency 1 selection
REG_4 - 'Frequency ALT2 select'	0x04	Alternate frequency 2 selection
REG_5 - 'Active frequency'	0x05	Read only – read the active frequency - Main/Alt1/Alt2
REG_6 - 'Sleep control'	0x06	Sleep mode selection and functionality
REG_96 - SIG100 UUID[47:40]	0x96	Read only - UUID[47:40]
REG_97 - SIG100 UUID[39:32]	0x97	Read only - UUID[39:32]
REG_98 - SIG100 UUID[31:24]	0x98	Read only - UUID[31:24]
REG_99 - SIG100 UUID[23:16]	0x99	Read only - UUID[23:16]
REG_9A- SIG100 UUID[15:8]	0x9A	Read only - UUID[15:8]
REG_9B - SIG100 UUID[7:0]	0x9B	Read only - UUID[7:0]

5.1 REG_0 - 'Device Control 0' (Address 0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	[0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]
Reserved	0	nLoopBack	Remote loopback	nAuto_Freq_change	Bitrate_sel[2:0]		

Bit [2:0] - Bitrate selection (see 3.4).

Bit [3] - nAuto_freq_change: '0' enables auto frequency change mode (see 3.4.4).

Bit [4] - Enable remote loopback mode (see 3.4.6).

Bit [5] - nLoopBack -Set this bit to disables loopback between HDI to HDO (see 3.4.5).

Bit [6] - '0'

Bit [7] - Reserved

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.2 REG_1 - 'Device Control 1' (Address 0x01)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	[0]	[0]	R/W [1]	[1]	[1]	[1]	[1]
Enable TXO high power	0	0	TX signal level	1	1	1	1

Bit [3:0] - '1111'

Bit [4] - TX signal level control at TXO pin: '0' - 1Vpp, '1' - 2Vpp (see 2.5.7).

Bit [6:5] - '00'

Bit [7] - Enable TXO high power. Set this bit to enable maximal TXO drive of 66mA, clear this bit for maximal TXO drive of 33mA (see 2.5.7).

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.3 REG_2 - 'Main Frequency Select' (Address 0x02)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
Main Carrier Frequency Configuration							

Bit [7:0] - Main Carrier Frequency configuration. Default configuration is 13MHz.

(See 3.4.3 - Carrier frequency configuration)

5.4 REG_3 - 'ALT 1 Frequency Select' (Address 0x03)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]	R/W [0]
Alternate Carrier Frequency 1 Configuration – ALT1							

Bit [7:0] - Alternate Carrier Frequency 1 configuration. Default configuration is 5MHz
(See section 3.4.3 Carrier frequency configuration).

5.5 REG_4 - 'ALT 2 Frequency Select' (Address 0x04)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]	R/W [1]	R/W [0]
Alternate Carrier Frequency 2 Configuration – ALT2							

Bit [7:0] - Alternate Carrier Frequency 2 configuration. Default configuration is 22MHz (See section 3.4.33.4.3).

5.6 REG_5 - 'Active Frequency Select' (Read-Only, Address 0x05)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
Current Active Carrier Frequency Configuration							

Bit [7:0] - Current Active Carrier Frequency (See section 3.4.33.4.3).

5.7 REG_6 - 'Sleep Control' (Address 0x06)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W [0]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [1]	R/W [0]	R/W [0]
Enter Sleep mode	Auto WUM	nAutoSleep	Long WUM	AutoSleep-timeout		Sleep modes selection	

Bit [1:0] '00' - Enhanced Sleep mode [SLP1],
'01' - Fast wake-up Sleep mode [SLP2],
'10' - Very low-power sleep mode [SLP3],
'11' - Deep Sleep mode [SLP4] (see section 4.3).

Bit [3:2] - AutoSleep-timeout - The time before entering into sleep mode (when AutoSleep mode is enabled). The duration is in seconds x 2 (i.e. default 6 sec), see 4.4.

Bit [4] - Wake-up message duration over the powerline (see Table 10).

Bit [6] - Auto wake-up message (WUM): '0' disables transmission of WUM upon NSLEEP pin wakeup.

Bit [7] - Enter Sleep mode reg. Activates the Sleep mode as selected in Bit [1:0] by setting bit[7]. Upon entering Sleep mode, bit [7] is automatically cleared to '0'.

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.8 REG_96 – UUID[47:40] (Address 0x96)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[47:40]							

Bits [7:0] - UUID[47:40]

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.9 REG_97 – UUID[39:32] (Address 0x97)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[39:32]							

Bits [7:0] - UUID[39:32]

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.10 REG_98 – UUID[31:24] (Address 0x98)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[31:24]							

Bits [7:0] - UUID[31:24]

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.11 REG_99 – UUID[23:16] (Address 0x99)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[23:16]							

Bits [7:0] - UUID[23:16]

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.12 REG_9A – UUID[15:8] (Address 0x9A)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[15:8]							

Bits [7:0] - UUID[15:8]

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.13 REG_9B – UUID[7:0] (Address 0x9B)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
R	R	R	R	R	R	R	R
UUID[7:0]							

Bits [7:0] - UUID[7:0]

R - Readable bit, W - Writeable bit [x] - Value on power up. '1' - bit is set; '0' - bit is cleared

5.14 Registers configuration (Command mode)

The Command mode allows the ECU to access the SIG100 internal registers for write and read operations. Enter the Command mode by lowering the HDC pin. During Command mode, the SIG100 is in *Soft-Reset* state. The device powerline communication is disabled. Every register configuration is kept until the next power-up/reset event.

During command mode, the SIG100 will automatically learn the Host bitrate regardless SIG100 configured bitrate. When exiting the command mode to normal mode, the SIG100 returns to its configured bitrate. This way, the host does not need to switch to SIG100 bitrate during configuration mode.

For example, upon hard-reset/ power-up , the default SIG100 bitrate is 19.2kbit/s. Host bitrate is set to 115.2 kbit/s. Host can configure the SIG100 bitrate REG_0[2:0] using 115.2kbit/s bitrate during configuration. When returning to normal mode, the SIG100 will be configured to 115.2kbit/s until next hard-reset/power-cycle.

5.14.1 WRITE-REG command

Write register command consist of three bytes as described in Table 14.

Table 14 - WRITE-REG command structure

1 st Byte	2 nd Byte	3 rd Byte
0xF5	Register address	Data to write

1st byte, 0xF5, is the write command byte.

2nd byte is the designated register address to write to.

3rd byte is the data byte value to be written.

For example, writing 0x34 to REG_3 (address 0x03) preformed as follows:

1. Lower the HDC pin (Enter Command mode).
2. Wait at least 100nsec
3. Transfer 3 bytes: [0xF5][0x03][0x34] - The value 0x34 is written to REG_3.
4. Wait at least 100ns.
5. Raise the HDC pin (Exit Command mode to Normal mode).

5.14.1.1 Example 1 - WRITE-REG command

Figure 17 depicts a *WRITE-REG* command sequence. First, the HDC is pulled low and the device enters the Command mode. The ECU sends the write command with 1st byte of 0xF5, followed by the control register address byte (A[7:0]) and the data byte to be written (B[7:0]). After completing the write sequence, the HDC pin pulled high and the device returns to Normal mode.

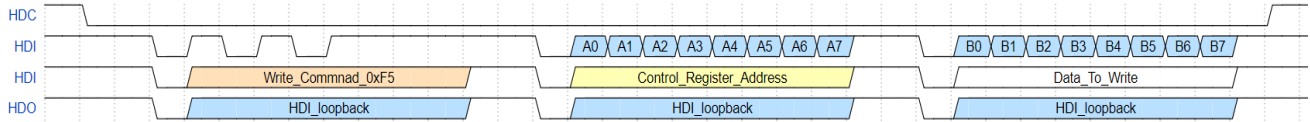


Figure 17- WRITE-REG command sequence

5.14.2 READ-REG command

A READ-REG command consist of 2 bytes as described in Table 15.

Table 15 - READ-REG command structure

1 st Byte	2 nd Byte
0xFD	Register address

1st byte, 0xFD, is the Read command byte.

2nd byte is the designated register address to read from.

Following the second byte, the SIG100 outputs the register value to ECU.

For example, reading from REG_5 (address 0x05) is performed as follows:

1. Lower the HDC pin (Enter Command mode).
2. Wait at least 100nsec
3. Transfer 2 bytes: [0xFD][0x05]
4. Wait for the SIG100 to output the value of REG_5.
5. Wait at least 100ns.
6. Raise the HDC pin (Exit Command mode to Normal mode).

5.14.2.1 Example 2 - READ-REG command

Figure 18 depicts a *READ-REG* command sequence. First, the HDC is pulled low and the device enters the Command mode. The ECU sends the read command with 1st byte of 0xFD, followed by the control register address byte (A[7:0]). Then the ECU receives the register internal value (B[7:0]). The HDC pulled back to high and the device returns to Normal mode.

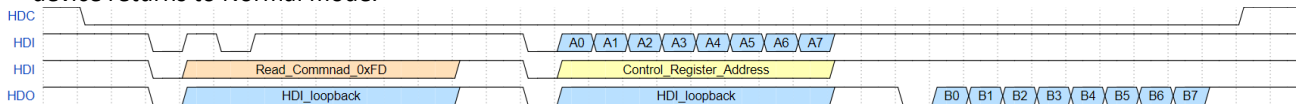


Figure 18 – READ-REG command sequence

6. Specifications

Table 16 - Absolute maximal rating

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Input voltage, DC	V_{im}		-0.6	3.3	3.9	V
Output voltage, DC	V_{om}		-0.6	3.3	3.9	V
Ambient temperature	T_{am}		-40		125	°C
Storage temperature	T_{sm}		-55		150	°C

Table 17 - Recommended operation conditions

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DVCC} V_{AVCC}		3.0	3.3	3.6	V
Supply Voltage ripple	V_{CC_RIP} A_{VCC_RIP}	Max 2.5MHz, waveform type of triangular		50m		V-p-p
Ambient operating temperature range	T_A		-40		105	°C
Minimum high level input voltage	V_{IH}		2			V
Maximum low level input voltage	V_{IL}				0.8	V
Minimum high level output voltage	V_{OH}		2.4			V
Maximum low level output voltage	V_{OL}				0.4	V
Maximal output current	I_{out}	see Table 1				
Maximum input current	I_{IN}		-1		1	μA

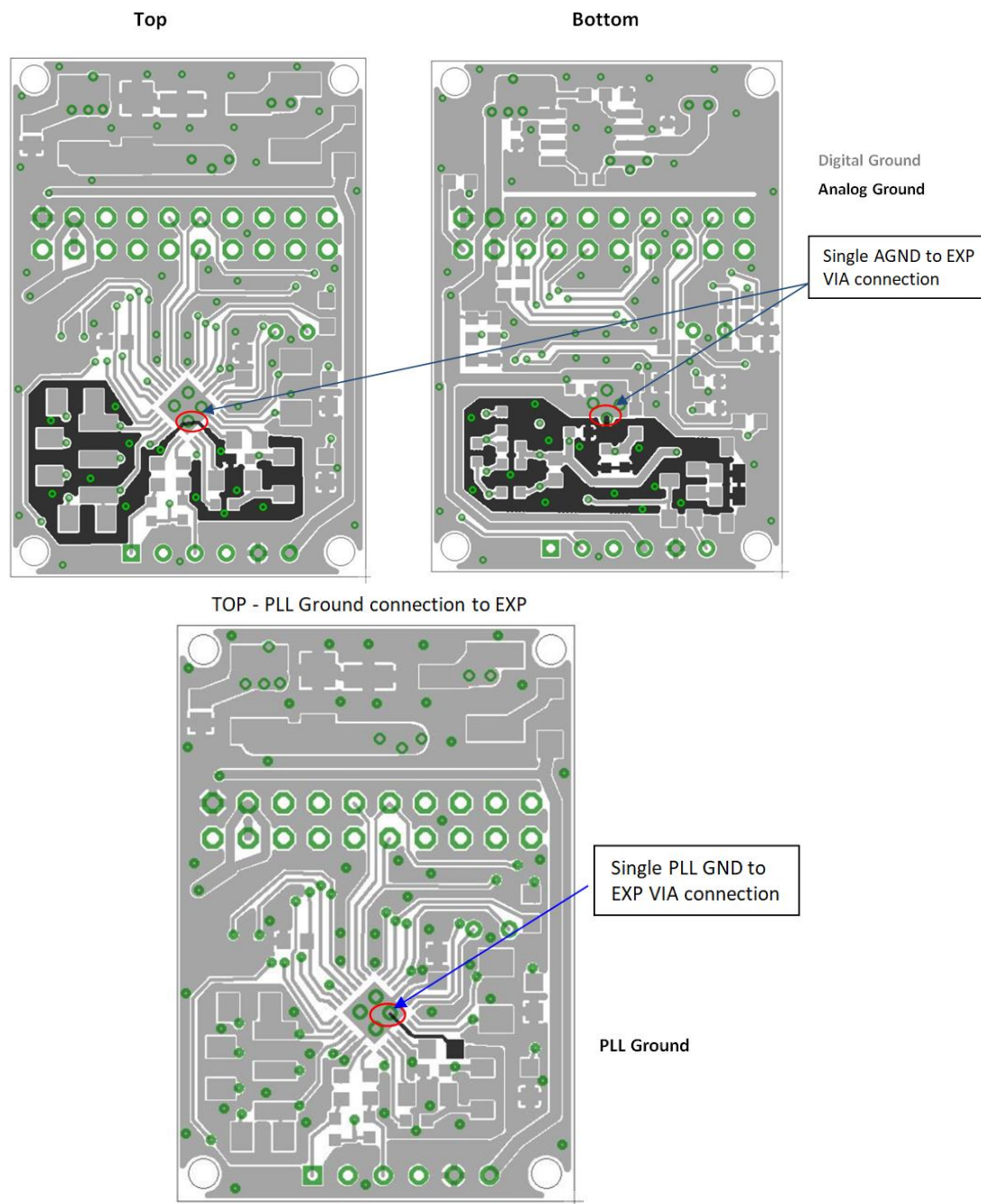
Table 18 - Device characteristics

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Extrnal componenets requierments						
Powerline coupling capacitor	C _{coupling}	Capacitor voltage rate should be selected with respect to powerline voltage	1.0	2.2	2.4	nF
Protection diodes capacitance	D _{protec}				10	pF
Capacitor at VCAP	V _{cap}		1	4.7		μF
Capacitor at PLLCAP	PLL _{cap}		1			μF
Capacitor at VREF	VREF _{cap}		1			μF
Inductor at L1	L1	see 2.5.4		3.3 / 18		μH
Inductor at L2	L2			15		μH
L1 pin input capacitance					1	pF
Crystal frequency	Xtal _{freq}	see2.5.2 2.5.2		16		MHz
Crystal frequency tolerance	Xtal _{ppm}				50	±ppm
AC signals charactetricts						
Tx signal at TXO	TXO _{lev}	TXON high (transmission is active) see 2.5.7	1		2	V-p-p
TXO input impendace	TXO _{in}	TXON low (transmission is not active)	200k			Ω
TXO output impedance	TXO _{out}	TXON high (transmission is active)		18		Ω

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
TXO driving current	I_{TXO}	TXON high (transmission is active)	33		66	mA
Rx signal at RXI	RXI_{lev}		10m		3.3	V-p-p
RXI input impedance	RXI_{In}		5.1k			Ω
Carrier Frequency in-band (channels selection)	F_c	Selection resolution is 100kHz, total of 251 carrier frequencies, see 3.4.3	5		30	MHz
Adjucent channels spacing	F_{adj}	The space between two adjucent channels operating over same powerline.	1			MHz
Timing requierments of UART/LIN interface						
UART bitrate	$UART_{br}$	ECU UART bitrate, see 3.4	9.6		115.2	kbit/s
Powerline latency	T_{RX_delay}	The delay from ECU start bit transmission to ECU start bit reception.		2.5		T_{bit}
Powerline PLC-byte length	T_{pl_byte}			10		T_{bit}
Timing of device operation modes						
Power-up/ hard-reset	T_{init}	Initialization time after power-up or hard-reset event.		2		ms
Carrier frequency change	T_{freq_cng}	Carrier frequency change process time		1		ms
Current Consumtption @ 3.3V						
Normal TX mode	I_{Tx}	TXON high (transmission is active)		65		mA
Normal RX mode	I_{RX}	TXON low (transmission is not active)		30		mA

7. SIG100 PCB layout recommendation

Note: Analog ground layer and GND PLL should be connected to the digital ground near the Exp pad.

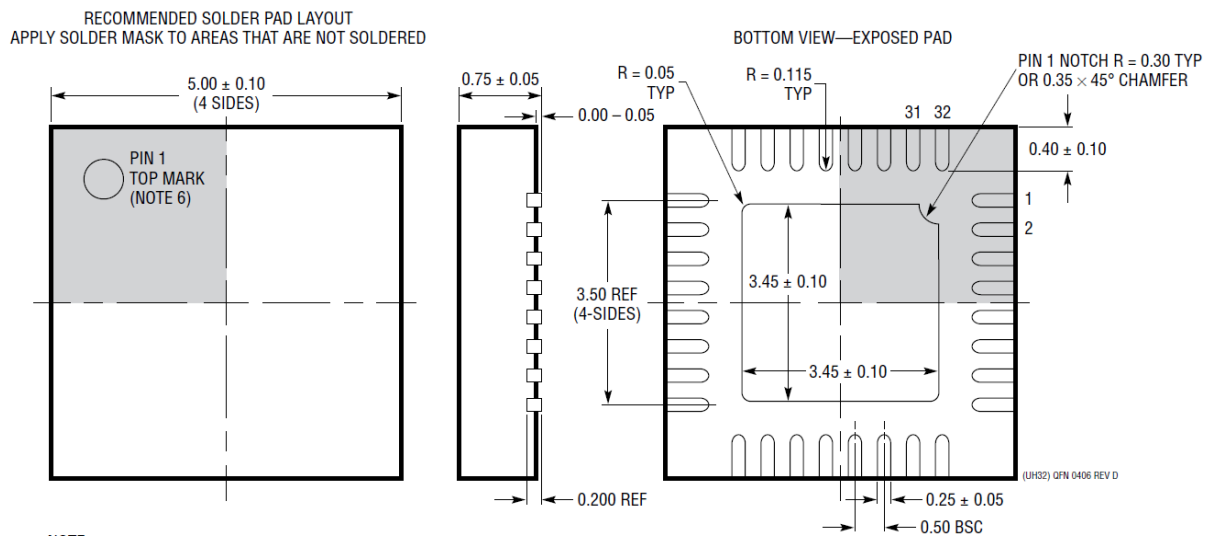


- ✓ VCC and DGND layout traces should be as wide as possible. Connect a 0.1uF capacitor between each VCC and DGND pins, as close as possible to the pins.
- ✓ Connect AGND to EXP with a single short trace.
- ✓ Connect PLL_GND to EXP with a single short trace.
- ✓ Connect L1, L2, C3, C5, C7, C8, C11, and C12 as close as possible to their pins.
- ✓ Connect R1 as close as possible to RXI pin.
- ✓ Connect all filtering capacitors as close as possible to their pins.
- ✓ Connect crystal and its capacitors close to OSCI and OSCO pins. Keep DGND plan around them.

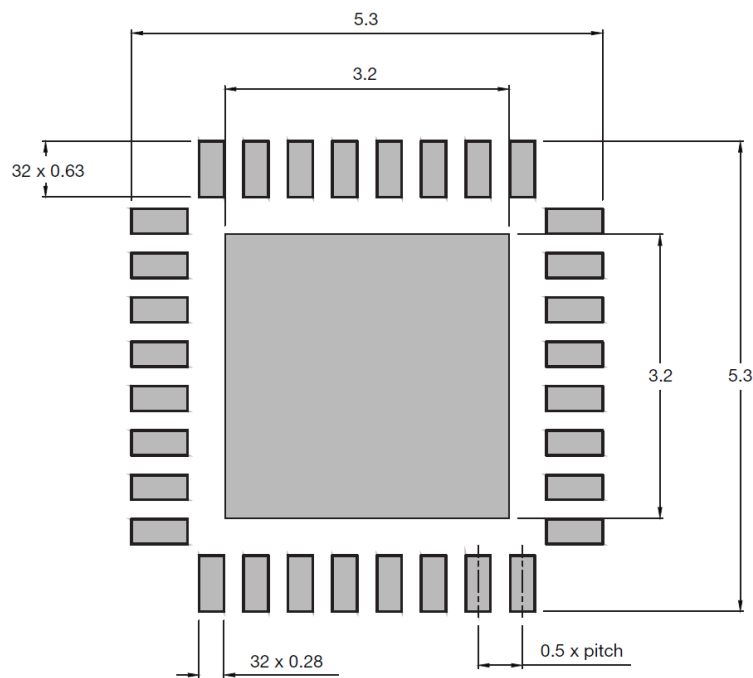
8. Package, Mechanical

The SIG100 package is QFN 32 5mm x 5mm.

8.1 Mechanical Drawing



8.2 PCB drawing



8.3 Soldering profile

Soldering reflow profile is according to IPC/JEDEC J-STD-020 (MSL3).

- Peak temperature (TP) is 260°C .
- Holding time is between 60 sec to 120 sec between TH min 150°C to TH max 200°C .
- Liquidus temperature (TL) is 217°C . Liquidus time is between 60 sec to 150 sec.
- TL to TP max ramp up is $3^\circ\text{C}/\text{sec}$.
- TP to TL max cool down rate is $6^\circ\text{C}/\text{sec}$.
- Max time above 255°C (T_p) is 30 sec.

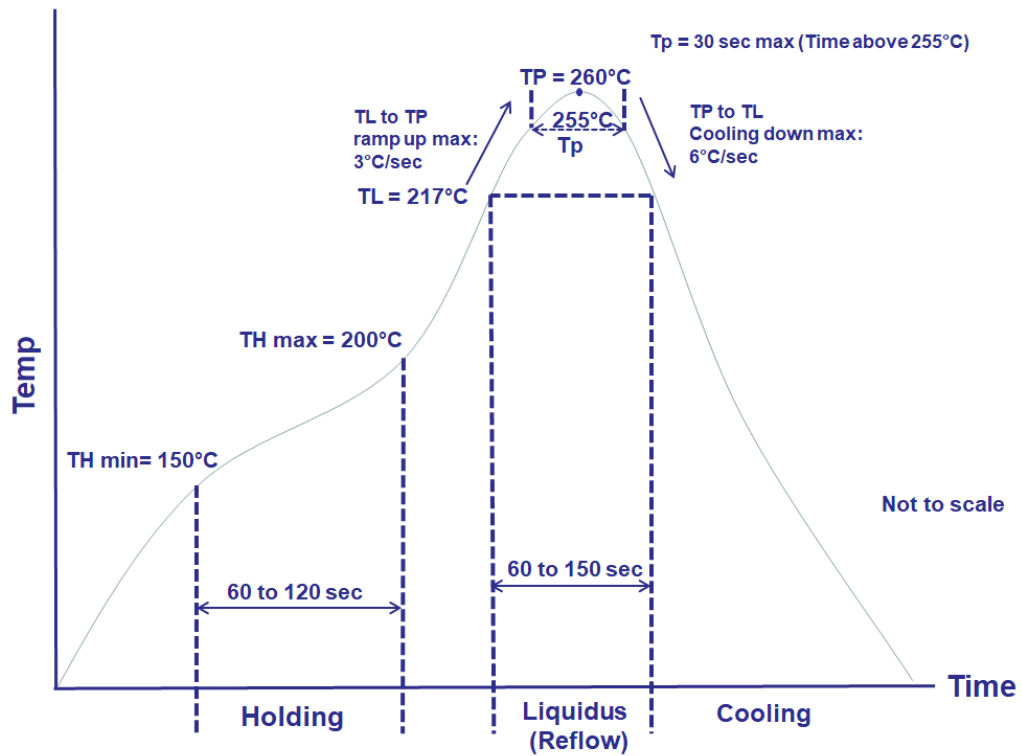


Figure 19 – Representation of IPC/JEDEC J-STD-020 (MSL3) profile

9. Test Environment

Figure 20 depicts the DC-BUS Test environment that allows testing the SIG100 devices in Lab emulated DC powerline attenuation environment.

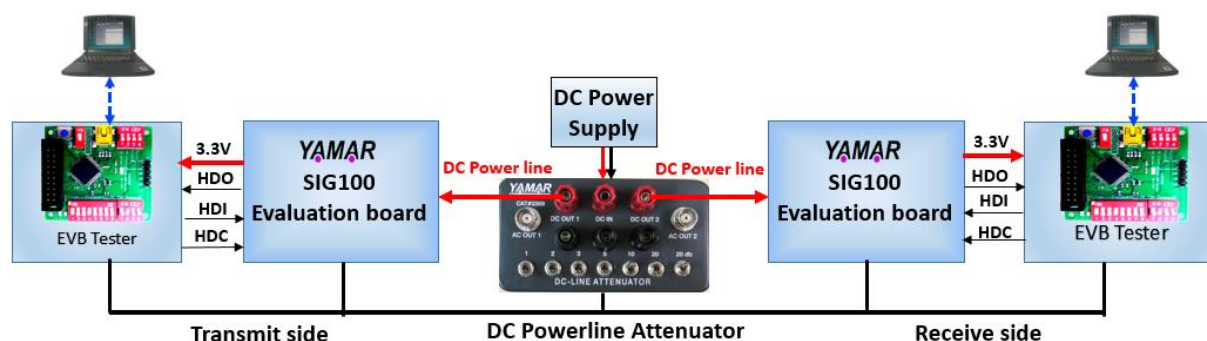


Figure 20 - DC-BUS Test environment

This test environment consists of two SIG100 evaluation boards (EVB), two EVB Testers and PC Test Program. The DC-Powerline Attenuator is an optional.

At the transmitting side, when the USB interface is not connected to a PC, it can generate repeatedly a predefined test message [A B C ...X Y Z] saving the need for a second PC. At the receiver side, the received test message is transferred from the EVB through the USB interface to a PC. The Test program analyze the received predefined messages and preform BER statistics including error byte, missed byte, and noise byte counting indications.

The DC-powerline attenuator is used to test the communication performance in variable attenuation levels (0-61dB), emulating a DC powerline environment. When connecting the EVB directly to a power supply, it is recommended to add in serial to the power supply an inductor (>22uH) to avoid strong attenuation due to power-supply's input filtering capacitors.

Revision History

Rev.	Date	Description
0.73	20/05/2019	Initial preliminary revision.
0.74	2/8/2019	Rearrange paragraphs
0.75	2/9/2019	Update schematics, Table 18.
0.76	23/09/2019	Editing.
0.77	02/10/2019	Update Table 3 and Figure 7.
0.78	14/11/2019	Update Figure 5 and NSLEEP pin description.
0.79	19/01/2020	Update Table 3.
0.80	19/02/2020	Update clause 2.5.3. Add UUID clause 3.4.7 Update clause 5 with UUID REGs.
0.81	21/04/2020	Add soldering profile description in section 8.3.



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深圳市南频科技有限公司

D-Win Technology (HongKong) Co., Ltd